DESIGN AND SIMULATION OF ANALOG CIRCUITS FOR ADAPTIVE RESONANCE THEORY (ART) NEURAL NETWORKS

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Introduction:

There are two prominent adaptive resonance theory (ART) neural network architectures: the ART1 and the ART2 [1]. Both architectures are capable in classifying an arbitrary set of input patterns into different categories. The categories are formed based on the similarities of the input patterns presented to the network. The ART1 neural network can classify in the parallel manner an arbitrary set of binary input patterns into different categories [2], thus making it very attractive for high-speed signal processing applications such as image and pattern recognition. The ART1 neural network consists of two layers of nodes denoted by F1 and F2. The nodes in the F1 layer are completely interconnected with the nodes in the F2 layers, and vice versa. Furthermore, the nodes in the F2 layer are completely interconnected with each other. The ART1 can only respond to binary inputs whereas the ART2 can respond to binary as well as analog inputs. One of the advantages of the ART1 architecture is its ability to perform in real-time or on-line (without requiring external control or supervision) when it is implemented in hardware [3].

Objective:

In this paper we design and simulate an analog integrated circuit which performs the same functionality as the ART1 neural network. The neural network incorporates both F1 and F2 layers in conjunction with their interconnections. Our circuit design is based on operational amplifiers which are relatively inexpensive and have been widely used in many circuit applications. Figure 1 shows the one-node circuit of the ART1 neural network (the triangles in the circuit represent operational amplifiers). This circuit is used as the primitive cell for constructing the complete 13-node ART1 system (four F1-layer nodes, eight F2-layer nodes, and one control node), as shown in Fig. 2. The circuits designed will be verified using Pspice, a circuit simulator run on a Sun SPARC II workstation. Comparisons will also be made between the Pspice simulations and the results obtained from solving the differential equations.

Some Results:

Fig. 3 shows the simulated transient responses taken at four different outputs of the complete 13-node ART1 system. These results are in excellent agreement with those calculated directly from the coupled different equations governing the ART1 neural network.

Detailed simulation results and comparisons will be presented in the Symposium.

References

[1] S. Grossberg, "Nonlinear neural networks: principles mechanisms and architectures," Neural Networks, vol. 1, pp. 17, 1988.

[2] G. A. Carpenter and S. Grossberg, "A massive parallel architecture for a self-organizing neural pattern recognition machine," Computer Vision, Graphics, and Image Proc., vol. 37, pp. 54, 1987.

[3] S. W. Tsay and R. W. Newcomb, "VLSI implementation of ART1 memories," IEEE Trans. Neural Networks, vol. 2, pp. 214, 1991.

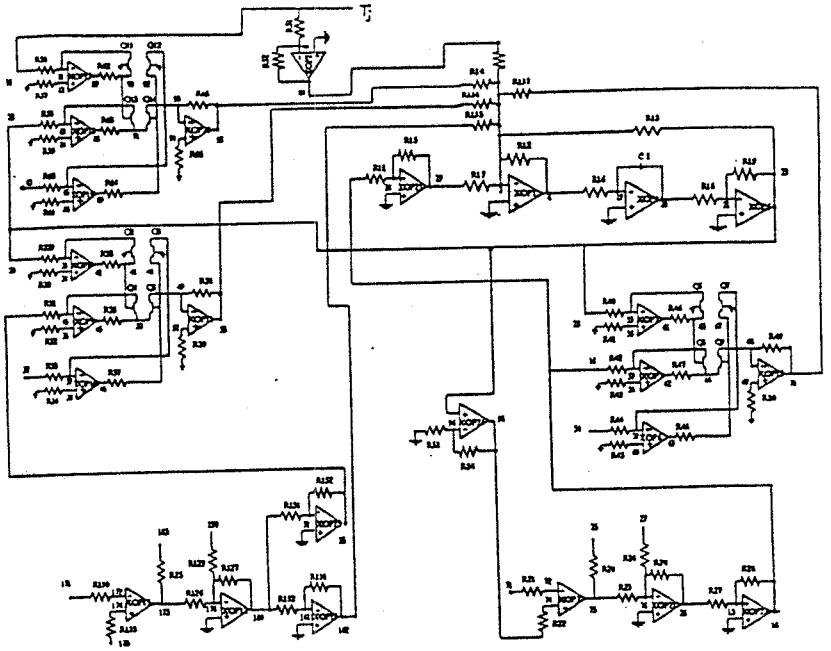

Figure 1: One-node circuit of the ART1 neural network

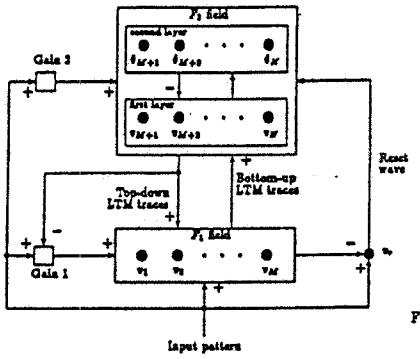

Figure 2: The architecture of the augmented ART1 neural network model.

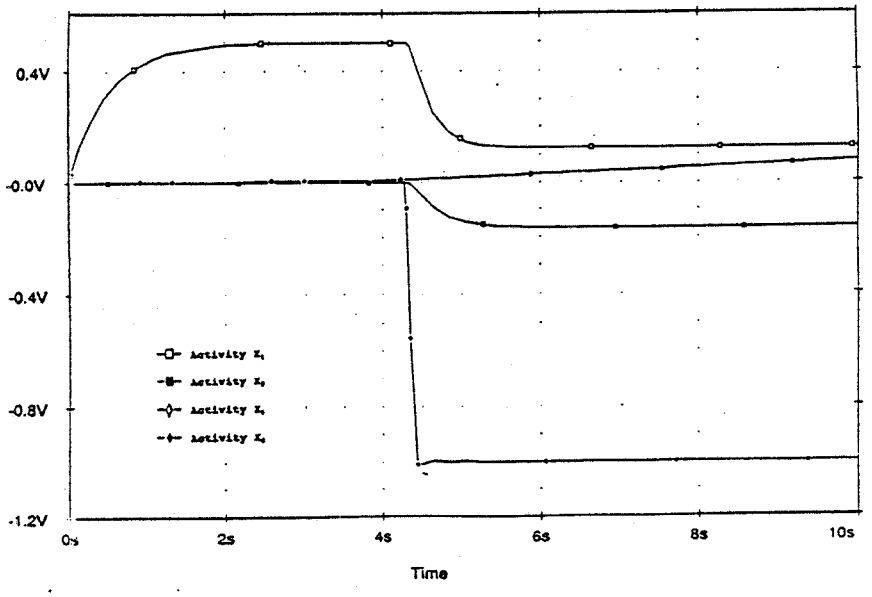

Fig-3. PSpice simulation results for a four-node neural network in the pattern I'=1000: X_1 and X_2 are the activities of node 1 and node 2 in the F_1 layer, and X_5 and X_6 are the activities of node 5 and node 6 in the F_2 layer, respectively.