FPGA 2015: Call for Papers

Twenty-Third ACM/SIGDA International Symposium on Field-Programmable Gate Arrays
February 22 - 24, 2015
Monterey, CA

http://www.eecs.ucf.edu/isfpga/

Submission Deadline: ~~Sept. 22, 2014~~

September 29, 2014 (Newly Extended!)

The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays is the premier conference for presentation of advances in all areas related to FPGA technology. For FPGA 2015, we are soliciting original submissions describing novel research and developments in the following (and related) areas of interest:

- **FPGA Architecture:** Novel logic block architectures, combination of FPGA fabric and system blocks (DSP, processors, memories, etc.), design of routing fabric, I/O interfaces, new commercial architectures and architectural features.
- **FPGA Circuit Design:** Novel FPGA circuits and circuit-level techniques, impact of process and design technologies, methods for analyzing and improving issues with soft-errors, leakage, static and dynamic power, clocking, power grid, yield, manufacturability, reliability, test; studies on future device technologies (e.g. nano-scale, 3D gate) for FPGAs.
- **CAD for FPGAs:** Placement, routing, re-timing, logic optimization, technology mapping, system-level partitioning, logic generators, testing and verification, CAD for FPGA-based accelerators, CAD for incremental FPGA design and on- line design mapping and optimization, CAD for modeling, analysis and optimization of timing and power.
- **High-Level Abstractions and Tools for FPGAs:** General-purpose and domain-specific models, languages, tools, and techniques to facilitate the design, development, debugging, verification, and deployment of large-scale and high-performance FPGA-based applications and systems - e.g. hardware/software co-design, high-level synthesis, SystemC virtual platform, DSP, compute acceleration, networking or embedded system tools and methodologies.
- **FPGA-Based and FPGA-like Computing Engines:** Compiled accelerators, reconfigurable computing, adaptive computing devices, systems and software, rapid-prototyping.
- **Applications and Design Studies:** Implementation of novel designs on FPGAs to achieve high-performance, low-power, or high-reliability, making use of the unique flexibility provided by FPGA architectures. Application-domain studies to analyze or improve FPGA architectures and implementations for networking, DSP, embedded, audio/video, automotive, imaging and other relevant areas.

Optimization of FPGA-based cores (e.g. arithmetic, DSP, security, embedded processors, memory interfaces, or other functions).

- **Panel Outlines:** Topic proposals for the traditional Monday night Panel Session at FPGA.

This year, we will start a new Designers Track. We solicit paper submissions providing tutorials and design experiences on known-interesting topics describing effective design techniques, design flows, methods, and new tool features. The submissions will be in a short-paper format, with at most 4 pages. These submissions will be reviewed by a separate group of reviewers with rich design and industrial experiences. This new track will lead to a full-day event on Sunday (Feb. 22), to bring FPGA users, designers, experts, consultants, and researchers together to share design experiences and learn new design solutions. To submit to this track, please select Design/Tutorial Paper under Submission Type.

Authors are invited to submit English language PDF of their paper or panel proposal by September 29, 2014 11:59 PM anywhere on Earth. Submitted papers will be considered for acceptance as a full paper (10 pages maximum), as a short paper (4 pages), as a design/tutorial paper (4 pages maximum), or as a poster.

The FPGA Symposium uses a double-blind reviewing system. Manuscripts must not identify authors or their affiliations. Self-references can either (1) be shown as "Removed for blind review" or (2) be referenced in the 3rd person, in the same way you would reference work by another group. Papers that identify authors will not be considered. Exceptions may be made for papers presenting new FPGA-related community infrastructure if the ability of reviewers to access that infrastructure is key to evaluating the paper. Please contact the Program Chair before submitting if you feel that it is not possible to avoid identifying the paper authors.

Papers should be submitted on-line to: http://www.eecs.ucf.edu/isfpga/

All papers should use the ACM formatting templates available at: http://www.acm.org/sigs/pubs/proceed/template.html

Notification of acceptance will be sent by mid-November. The authors of accepted papers will be required to submit the final camera-ready copy by early December. Proceedings of the accepted papers will be published by ACM and included in the ACM Digital Library.

Address questions about the technical program to:

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Address general questions about the conference to

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