UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Spring 2015 Seminar Series

Presented by the ECE Division

Parallelism for High Performance Data Processing: a rethinking

Thursday, February 12th, 2015
10:30 AM - HEC 450

Scalable data management for big data applications is a challenging task. It puts even more pressure on the lasting memory-wall problem, which makes data access the prominent performance bottleneck for high performance computing (HPC), and has changed the interest of HPC to HPDP (High Performance Data Processing). HPC is known for its massively parallel architectures. A natural way to achieve HPDP is to increase and utilize memory concurrency to a level commensurate with that of HPC. We argue that substantial memory concurrency exists at each layer of current memory systems, but it has not been fully utilized. In this talk we reevaluate memory systems and introduce the novel C-AMAT model for system design analysis of concurrent data accesses. C-AMAT is a paradigm shift to support sustained data accessing from a data-centric view. The power of C-AMAT is that it has opened new directions to reduce data access delay. In an ideal parallel memory system, the system will explicitly express and utilize parallel data accesses. This awareness is largely missing from current memory systems and missing from current architecture and algorithm design. We will review the concurrency available in modern memory systems, present the concept of C-AMAT, and discuss the considerations and possibility of optimizing parallel data access for big data applications. We will also present some of our recent results which quantize and utilize parallel I/O following the parallel memory concept for HPDP.

Dr. Xian-He Sun
Illinois Institute of Technology

Dr. Xian-He Sun is a Distinguished Professor of Computer Science of the Department of Computer Science at the Illinois Institute of Technology (IIT). He is the director of the Scalable Computing Software laboratory at IIT and a guest faculty in the Mathematics and Computer Science Division at the Argonne National Laboratory. Before joining IIT, he worked at DoE Ames National Laboratory, at ICASE, NASA Langley Research Center, at Louisiana State University, Baton Rouge, and was an ASEE fellow at Navy Research Laboratories. Dr. Sun is an IEEE fellow and is known for his memory-bounded speedup model, also called Sun-Ni's Law, for scalable computing. His research interests include parallel and distributed processing, memory and I/O systems, software systems for big data applications, and performance evaluation. He has over 200 publications and 5 patents in these areas. He is a former IEEE CS distinguished speaker, a former vice chair of the IEEE Technical Committee on Scalable Computing, the past chair of the Computer Science Department at IIT (9/2009-8/2014), and is serving and served on the editorial board of most of the leading professional journals in the field of parallel processing. More information about Dr. Sun can be found at his web site www.cs.iit.edu/~sun/.