UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Fall 2014 Seminar Series

Presented by the ECE Division

ASSET-BASED STRUCTURAL CHECKING FOR HARDWARE TROJAN DETECTION IN SOFT IPs

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11:00 AM – HEC 101

As the impacts of malicious insertions in hardware (i.e., hardware Trojans) attract more and more attentions from government and industry, methodologies and tools are needed to detect such insertions at various steps in the IC design flow. This presentation introduces a developing technology, named Structural Checking, which screens RT-level digital hardware designs for suspicious logic. Structural Checking is based on signal assets, which indicate the contribution of a signal to the system. By assigning and filtering assets throughout the design, Structural Checking tool is able to analyze the circuit for identifying abnormal asset patterns on signal paths, and alerts user for further inspection. While avoiding complex functionality analysis and focusing on circuit structure, Structural Checking allows for hardware Trojan detection in earlier phase of IC design, which may also work with other malicious insertion detection methods at various levels of abstraction.

Jia Di

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Dr. Jia Di received B.S. and M.S. degrees from Tsinghua University, China, in 1997 and 2000, respectively. He completed his Ph.D. in Electrical Engineering at the University of Central Florida in 2004. He then joined the Computer Science and Computer Engineering Department of the University of Arkansas in August 2004, where he is now a Professor. His research area is asynchronous integrated circuit design for applications including extreme temperature, ultra-low power, radiation hardening, and hardware security. His Trustable Logic Circuit Design (TruLogic) Lab, which consists of 15 Ph.D. and M.S. students, has been well sponsored by various federal agencies and industry. The TruLogic Lab tapes out multiple ICs every year for validating their circuit designs. Dr. Di has published one book and a number of research papers on technical journals and conferences. He also has two U.S. patents. Dr. Di is a senior member of IEEE and a member of the National Academy of Inventors. He is an associate editor of Journal of Low Power Electronics (JOLPE).

Hosted by: Dr. Jiann-Shiun Yuan