UCF DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Spring 2016 Seminar Series

FROM EMERGING MEMORIES TO NOVEL ARCHITECTURES AND NEW FUNCTIONALITIES

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With CMOS approaching the end of conventional scaling, many novel switches have been proposed and experimentally explored for beyond-CMOS applications; however, all these switches still face numerous challenges and tradeoffs. At the same time, intriguing research opportunities arise across boundaries, e.g., between logic and memory, between devices and architectures, etc.

Emerging memories offer several promising candidates for next-generation memory, storage, and computing solutions, e.g., phase change memory (PCM), spin-transfer-torque random-access-memory (STTRAM), resistive RAM (RRAM), etc. Significant progress has been made on all these technologies, although challenges still exist. RRAM has poor reliability and large variability due to its stochastic mechanisms, which needs to be improved through oxide stack engineering, operation control, and design technology co-optimization. STTRAM has the fastest speed and longest endurance among emerging memories for high-performance applications, but next-generation technology may require new physical mechanisms for more efficient and more reliable STTRAM cell design. There are promising research opportunities in the application-specific optimization of these emerging memory technologies.

Most emerging memories have two-terminal structures and are suitable for crossbar arrays where the large number of sneak paths present a major challenge. Two-terminal selectors with nonlinearity or asymmetry may suppress sneak leakage, which include rectifying diodes, nonlinear devices, and volatile switches. Crossbar array analysis and selector device assessment require a comprehensive model that incorporates various design and technology parameters. With high device density, structural regularity, and intrinsic parallelism, crossbar arrays also have promising applications beyond memory space, e.g., programmable logic, non-Boolean computing, synaptic network, etc.

The research on emerging memories and selector devices provides a technology platform to explore new functionalities and novel architectures. The analog behaviors of emerging memories can be utilized to imitate synaptic weight modulation in neural network for neuromorphic computing. The randomness in some emerging memory characteristics can be exploited to generate hardware security primitives. Emerging devices (including memories) provide some unique characteristics unavailable in digital CMOS, which may be better utilized in novel architectures beyond CMOS. Novel architectures and computing solutions may also require emerging devices for more efficient implementation. Therefore, there are tremendous opportunities to bridge the research gap between emerging devices and architectures. Emerging memories and memory-centric architectures present a good example to utilize nonvolatility and scalability of memory devices in novel architectures. These novel functionalities and architectures may enable more efficient, intelligent, and secure nanoelectronic systems.

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An Chen received his Ph.D. degree in Electrical Engineering from Yale University in 2004. An started working on emerging memory technologies at Spansion LLC. In 2007, he joined AMD as a full-time assignee to the Nanoelectronics Research Initiative (NRI) program with SRC. He continued working on beyond-CMOS devices with the NRI and STARnet programs at GLOBALFOUNDRIES, which separated from AMD in 2009. He is also the Memory Tech Lead responsible for research collaborations with industry consortia and partners on emerging memories. Since 2011, An has been the chair of the Emerging Research Device (ERD) group of the International Technology Roadmap for Semiconductors (ITRS). An has published 38 first-author and 7 co-author papers in peer-review journal and conference proceedings. He holds 16 issued U.S. patents and 4 pending applications. He has presented over 20 contributed talks and over 30 invited talks and panel discussions in conferences. He is the lead editor of "Emerging Nanoelectronic Devices" (Wiley, 2015) and has contributed chapters to four books. He is on the Advisory Boards of the University of Nebraska - Lincoln MRSEC center and the University of Florida Nanoscale Security MURI program, and has also served in the Technical Advisory Board of several SRC programs and thrusts. An is a Senior Member of IEEE.