Low-power embedded computing and high-performance computing are pervasive and important in various scales of applications, ranging from battery-powered embedded systems, handheld smartphones, desktop computers and household appliances, to data centers and grid-level applications. In my talk, I will discuss my work on near-threshold computing for low-power embedded systems with next-generation technologies. We investigate the characteristics of FinFET devices and circuits, and optimize the structure of FinFET circuits and systems under near-threshold computing. We propose a device-circuit-architecture cross-layer design framework, starting from accurate FinFET device modeling, logic and memory cell optimization, to performance and energy efficiency enhancement techniques.

In high-performance data centers, over-provisioning of energy storage devices (ESDs) provides new opportunities for performing power capping and capex/opex reduction without performance degradation. We propose the hierarchical ESD structure for data centers and the corresponding provisioning and control framework for design-time optimization and run-time control. I also work on future data center structure and propose the data-center-on-a-chip (DCoC) paradigm. We solve the virtual machine mapping problem in the DCoC paradigm to minimize the communication cost while satisfying chip power budget and power density constraints.

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