Since the early 2000s, power has been the central problem that limits the performance of computer systems, from datacenters to smartphones and wearable devices. Data movement is the primary contributor to power dissipation in nanometer ICs. Consider, for instance, the energy cost of performing a double precision addition on a graphics processing unit (GPU) implemented at the 22nm technology node: the energy required to fetch the two operands from memory is 50x greater than the energy required to move the operands from the edge of the GPU chip to its center, which itself is another 10x higher than the cost of the actual addition. This gap between the energy cost of data movement and computation is expected to widen in future computers. Thus, minimizing data movement is a first order design constraint for future computer systems.

In this talk, I will examine the first fully programmable DDRx controller that enables application specific optimizations for more energy and bandwidth efficient data movement between the processor and main memory. I will then present the memristive Boltzmann machine, a novel hardware accelerator that leverages in situ computation with RRAM technology to eliminate unnecessary data movement on combinatorial optimization and deep learning workloads. I will also overview a new data exchange mechanism using synchronized counters that enables energy efficient data movement in large last level caches.

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