UCF DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Spring 2016 Seminar Series

DIGITAL ENHANCEMENT TECHNIQUES FOR DATA CONVERTERS IN SCALED CMOS TECHNOLOGIES

FRIDAY JANUARY 29, 2016

2:00 PM – HEC 356

This talk presents digital enhancement techniques for data converters in advanced technology nodes. With technology scaling, traditional voltage-domain (VD) analog-to-digital converters (ADCs) face two major challenges: (1) reduction of dynamic range due to supply voltage scaling, and (2) decrease in intrinsic gain of transistors which makes high gain amplifier design tough. To address these challenges, a two-stage ADC architecture is presented which uses time-domain quantization to exploit the advantages of technology scaling. The architecture, consisting of a first stage successive approximation register (SAR) and a second stage ring oscillator, is highly digital and scaling friendly. A 40nm CMOS prototype achieves 75.7 dB dynamic range at an excellent Walden figure-of-merit of 18.5 fJ/conversion step. The proposed architecture has been extended to a capacitance-to-digital converter and a prototype has been developed in 40nm CMOS. The prototype can sense capacitances with a resolution of 1.3fF and has a Walden figure-of-merit of 55 fJ/step which is more than two times better than the current state-of-the-art.

This talk also presents digital techniques to improve performance of continuous-time(CT) ΔΣ digital-to-analog converters (DACs). Recently, CT ΔΣ DACs have received more attention than their discrete, switched-capacitor counterpart mainly because of low power and/or higher speed of operation. However, a critical disadvantage of CT ΔΣ DACs is their greatly increased sensitivity to inter-symbol interference (ISI) error. To address this shortcoming of CT DACs, this talk presents several algorithms that can mitigate ISI error simultaneously with static mismatch error. Further, the proposed algorithms are fully digital in nature and as such, are best poised to take maximum advantage of technology scaling.

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Arindam Sanyal received his PhD from The University of Texas at Austin in 2015 and his Masters from The Indian Institute of Technology, Kharagpur in 2009. He is currently working as a Design Engineer in the timing unit of Silicon Laboratories, Austin. His research interests are in data converter design with applications in bio-medical domain.