UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Spring 2015 Seminar Series

Presented by the ECE Division

NONVOLATILE MEMORY TECHNOLOGY BASED FUTURE MAIN MEMORY SYSTEM

TUESDAY MARCH 3, 2015

3:00 PM – HEC 450

Main memory scaling is in great peril as cell size remains constant and power consumption rises at the latest technology generation for traditional memory technologies, such as dynamic random access memory (DRAM). Recent innovations have identified emerging nonvolatile memories, such as phase change memory (PCM), as scalable solutions to boost memory capacity in a power efficient manner. Multi-level cell (MLC) PCM storing multiple bits in a single cell further increases storage density with a lower cost per bit. However, to deploy MLC PCM as a DRAM alternative and to exploit its scalability, MLC PCM must be architected to overcome its own disadvantages such as long write latency, short cell endurance and large write power. In this talk, I first will present write truncation to reduce the number of write iterations through error correction code. I will then describe elastic RESET that reduces write power and prolongs memory lifetime by triple levels cell and compression. At last, to reduce MLC PCM write power, I will propose RESET scheduling, which reduces the peak power within one write.

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Lei Jiang received his BS and MS from Shanghai Jiao Tong University China in 2006 and 2009, respectively. Lei completed his PhD in the University of Pittsburgh, 2014. He is working at AMD. His research topic includes phase change memory, STT-MRAM and Memristor. He is the co-recipient of the best paper award of the International Symposium on Low Power Electronics and Design (ISLPED) in 2013.

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