UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Spring 2015 Seminar Series

Presented by the ECE Division

ON-CHIP MEMORY CIRCUIT/ARCHITECTURE DESIGN ENABLING "MORE-THAN-MOORE" PARADIGM

Thursday, February 5th, 2015

1:30 PM - HEC 450

On-chip random access memory (RAM) area/capacity increases every technology generation in order to reduce accesses to external memories that require long latency and high energy consumption. However, large on-chip read only memories (ROM) have not been traditionally used, perhaps because of its limited usage and space availability. In this talk, I will show that conventional 6T SRAM bit-cell can store additional one bit of 'ROM' information by employing one extra word-line without area overhead or performance degradation on a bit-cell. Stability during the ROM mode is analyzed and architectural supports are proposed. As example applications, I will present fast evaluation of elementary mathematical functions and built-in self-test with high test quality. STT MRAM is considered as a promising future candidate for on-chip memory due to the attributes of non-volatility, zero stand-by leakage, and high density. Despite the promising attributes, designing high-density STT MRAM with low energy consumption is challenging. In the second part of my talk, I will present a new biasing method for STT MRAM that can reduce write time and write energy significantly. The proposed biasing method achieves the same switching time for P to AP transition and AP to P transition, and hence, energy/performance wastage induced by asymmetry between two transitions can be mitigated.

Dr. Dongsoo Lee

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Dongsoo Lee received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2002, 2004, and 2013, respectively. He was with Samsung Electronics, Ltd., Suwon, Korea, from 2004 to 2008, where he was involved in research on designing circuits for DTV one-chip solutions. In the summer of 2011, he worked as a graduate intern at Qualcomm Incorporated, San Diego, CA. In the summer of 2012, he worked as a graduate intern at Intel Corporation, Hillsboro, OR. He has been with IBM T. J. Watson Research Center as a Research Staff Member since July 2013. His current research interests include low power design, on-chip memory design, and processor design using emerging technology.

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