UCF | Electrical and Computer Engineering

Spring 2017 Seminar Series

Towards Efficient Integration of Emerging Non-Volatile Memory Technologies in Future Systems

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11:30 AM – HEC 450

With growing demand for larger memory capacities, compounded by the challenges of DRAM scaling, emerging Non-Volatile Memories (NVMs) present themselves as promising candidates for building future memory systems. Emerging NVMs, such as Intel and Micron's 3D XPoint, offer low access latency (comparable to DRAM), non-volatility, and high memory density. NVMs bring to the table the ability to build very large memory systems that merge storage and main memory into a single entity and consume almost zero idle power (no refresh power, unlike DRAMs). Nevertheless, designing systems with emerging NVMs is fraught with challenges. The most promising NVM technologies such as Phase-Change Memory (PCM), have limited write endurance and exhibit write operations that are both slow and power consuming. Additionally, non-volatility can expose security vulnerabilities such as data remanence attacks, making it extremely crucial to design strong security features into the architectures.

In this talk, I discuss the various opportunities and challenges of emerging NVMs and present solutions to some of these problems. The first part of the talk presents different techniques that enable efficient integration of emerging NVM technologies in future memory systems. The second part focuses on secure processor designs in the context of emerging NVMs. I conclude my talk by discussing some key research directions for practical deployment of emerging NVMs in future computing systems.

Amro J. Awad

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Dr. Amro Awad is currently a senior member of technical staff at Sandia National Laboratories. He completed his Ph.D. in Computer Engineering from North Carolina State University in Fall 2016. Since then, he has been working on researching, modeling, and evaluating future HPC systems at Sandia. Amro's PhD work was focused on enabling efficient integration of emerging NVM technologies in future systems. During his PhD, he interned at Los Alamos National Laboratory (LANL), HP Labs, and AMD Research. His research interests include computer architecture, emerging memory technologies, and hardware security.

Amro's research work has been accepted and published in multiple top-tier venues such as ISCA, HPCA, ASPLOS, ICS, and ISPASS. Moreover, Amro has served as a reviewer for multiple reputable computer architecture journals including TC, TVLSI, and CAL. He has also been invited to serve on the program committees for ISCA 2017 (EPC) and IISWC 2017 (PC) and has participated in multiple NSF review panels.