UCF | Electrical and Computer Engineering

# Spring 2018 Seminar Series

## Exascale Challenges

TUESDAY APRIL 3, 2018

12:30 PM – RB1-101

The need to move beyond petascale computing is driven at the national level because it affects scientific discovery, engineering, healthcare, security, and economic competitiveness. However, designing a machine that is 50x faster than today's peak of 20PF isn't as simple as building a machine 50x larger. At the node level, chip manufacturers are increasing transistor density rather than clock frequency and some manufacturers are pushing accelerators like GPUs and FPGAs as alternatives to traditional processors even though computation is quickly falling to the wayside as the bottleneck; memory is becoming the dominant factor in both energy and performance scalability. At the system level, engineers are faced with the problem of how to manage billions of messages passing through the network. These developments affect application and algorithm developers who must find ways to exploit all of this available parallelism. This talk will discuss these challenges and how they can be solved using a holistic approach to system and software engineering.

## Dr. Simon D. Hammond and Dr. Clay Hughes

### Sandia National Laboratories

**Simon D. Hammond** is a Principal Research Scientist in the Scalable Computer Architecture group at Sandia National Laboratories. His primary research focuses on enabling co-design activities for the laboratories using tools such as the Mantevo mini-application suite, the Structural Simulation Toolkit (SST), the Advanced Architecture test beds and several other projects. This work includes activities with the Office of Science Materials in Extreme Environments (ExMatEx) and Combustion (ExaCT) codesign centers as well as the Sandia NNSA Codesign project focused on large scale production-quality engineering applications and mathematical libraries. Since 2014 he has worked across the SIERRA and RAMSES production groups at Sandia to provide the first full production application ports to Intel's Knights Corner, Knights Landing and IBM's POWER8 processors. He continues to work closely with these teams to enable the Kokkos C++ programming model and porting to NVIDIA's GPUs, AMD's APUs and most recently Cavium's 64-bit ThunderX ARM processor. Additionally, he has research interests in high performance compilers (particularly vectorization strategies), dynamic runtimes with a focus on the just-in-time compilation and dynamic execution of code, the C++ language standard, efficient message passing, high performance numerical mathematics libraries and the analysis, modeling and optimization of large-scale parallel scientific or data analytics applications. Prior to joining to Sandia, Simon worked (during his PhD) in a UK Technology Transfer Partnership at the United Kingdom's Atomic Weapons Establishment (AWE).

**Clay Hughes** is a Senior Member of Technical Staff in the Scalable Computer Architecture group at Sandia National Laboratories. His responsibilities include support for co-design activities using the Structural Simulation Toolkit (SST) and the Heterogeneous Advanced Architecture Platforms. He is heavily involved in the Exascale Computing Project with PathForward and Hardware Technology. His background includes work on a detailed model of hardware transactional memory; development of dynamic power control and run-time scheduling for hardware transactional memory systems; development of a program-less input methodology for binary synthesis to study transactional memory; and the development of methods to reduce the simulation time for multi-threaded programs. Before joining Sandia, Clay was an Associate Teaching Professor at Florida State University where he supervised three M.S. students, taught undergraduate and graduate courses in computer architecture, ARM and MIPS assembly, real-time systems, and developed new courses in computer system design and embedded systems.

**4328 Scorpius Street Orlando, FL 32816**

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