



Electrical and Computer Engineering

Fall 2017 Seminar Series

Microarchitectural Adaptivity in High Performance CPUs

MONDAY NOVEMBER 13, 2017

11:00 AM – HEC 450

Modern microprocessors are extremely complex and leverage complex logic design to extract as much performance out of software applications as possible. Unfortunately, not all applications benefit from this complex design due to inherent limitations in their algorithm and the way they are coded. In such cases, the complex logic unnecessarily burns a lot of power to no good cause. Adaptive processor cores have the ability to dynamically adjust their execution resources to match the instruction-level parallelism (ILP) and memory-level parallelism (MLP) of different program phases. The goal of adaptivity is to maximize performance in as energy-efficient a manner as possible. In this talk, I will provide an overview of the adaptive microarchitecture landscape and examine the various ways adaptivity can be leveraged to make microprocessors better and more versatile. I will also discuss current and future research opportunities in this exciting direction.

Rangeen Basu Roy Chowdhury

Intel Corporation

Dr. Rangeen Basu Roy Chowdhury is a CPU Architect at Intel working on defining the next generation of Intel's core microarchitecture. The cores designed by his team are at the heart of all i-series, x-series and Xeon processors. Dr. Basu Roy Chowdhury received his B. Tech in Electrical and Computer Engineering from National Institute of Technology Durgapur, India and his Masters and PhD in Computer Engineering from North Carolina State University. He spent his early career designing high performance FPGA IPs for multi-gigabit 'Carrier Ethernet' switches. At North Carolina State University, he was part of the teams prototyping multiple proof-of-concept processors.

Dr. Basu Roy Chowdhury's past and current work has primarily revolved around microarchitectural techniques for improving energy efficiency of high performance micro-processors. He worked on adaptive processor microarchitecture and 3D-stacked heterogeneous multicore architecture during his PhD. His interests include CPU core microarchitecture, high performance memory systems, hardware-software co-design, design for X (X=test, reliability, debug etc.), and novel system architecture.

Hosted by: Dr. Amro Awad

4328 Scorpis Street Orlando, FL 32816

WWW.ECE.UCF.EDU