Electrical and Computer Engineering

Spring 2017 Seminar Series

Design, Measurement, and Modeling of High-Speed Interconnects

THURSDAY, MARCH 9, 2017

11:00 AM – HEC 450

High-speed interconnects are the fundamental components of modern computer and electronic devices/systems and have been a key determining factor in terms of performance, cost, form factor, and functionality. Interconnect technologies are critical enablers for addressing the expected future needs in terms of higher performance, lower costs, smaller form factors, more functionality, and/or higher security in computers, consumer electronics, communications, medical devices, and defense electronics, particularly as Moore's Law is slowing down. The designs, measurements, and modeling of interconnects are increasingly important in the developments of various computer and electronic products. This presentation focuses on several of our recent innovations for improving interconnects' designs, measurements, and modeling in computer systems. First, we will talk about an innovative absorbing termination technique and its applications to interconnect designs and measurements. The technique is used to mitigate stub effects in interconnects for high-speed signaling, and it can be utilized to reduce the complexity and lower the cost for high-frequency measurements. We will then discuss a new electronic design automation (EDA) technique, the broadband Green's function method, and its applications to fast electromagnetic modeling and simulations of interconnects. The method is faster by 2 to 3 orders in the analysis of printed circuit boards compared to conventional methods and commercial tools.

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Shaowu Huang earned his Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, in 2015. From 2012 to 2015, he worked as a signal integrity engineer at Intel Corporation. After leaving Intel, he joined Invensas Corporation, where he currently works on research and development of microelectronic packaging and interconnect technologies. He has published more than 60 journal and conference papers and filed more than 20 U.S. non-provisional patents. He has received the Intel High 5 Award and the Intel Distinguished Invention Award. He is member of the TC-9 and TC-10 committees of IEEE Electromagnetic Compatibility Society. He chaired the High Speed Link Design II session at the 2015 IEEE Symposium on EMC and signal integrity and the Computational Electromagnetics I session of the 2016 IEEE International Symposium on EMC.