

Electrical and Computer Engineering

Spring 2019 Seminar Series

Vanguard Astra: A Prototype Arm Supercomputer

THURSDAY Jan 24, 2019

2:00 PM - RB1-101

As part of its larger procurement strategy, the National Nuclear Security Administration (NNSA) commissioned the world's first ARM-based petescale supercomputer, Astra, which is deployed at Sandia National Laboratories. Astra is the first of a series of prototype systems for advanced architectures under the Department of Energy's Vanguard program, whose overarching goal is to expand the HPC ecosystem by testing and proving emerging technologies to determine their viability at scale. These technologies often have immature software stacks, so, in true co -design fashion, Vanguard seeks to address both hardware and software together. This talk will cover general system design, including both hardware and software, and early performance numbers.

Dr. Simon D. Hammond and Dr. Clay Hughes Sandia National Laboratories



Simon D. Hammond is a Principal Research Scientist in the Scalable Computer Architecture group at Sandia National Laboratories. His primary research focuses on enabling co-design activities for the laboratories using tools such as the Mantevo mini-application suite, the Structural Simulation Toolkit (SST), the Advanced Architecture test beds and several other projects. This work includes activities with the Office of Science Materials in Extreme Environments (ExMatEx) and Combustion (ExaCT) codesign centers as well as the Sandia NNSA Codesign project focused on large

scale production-quality engineering applications and mathematical libraries. Since 2014 he has worked across the SIERRA and RAM-SES production groups at Sandia to provide the first full production application ports to Intel's Knights Corner, Knights Landing and IBM's POWER8 processors. He continues to work closely with these teams to enable the Kokkos C++ programming model and porting to NVIDIA's GPUs, AMD's APUs and most recently Cavium's 64-bit ThunderX ARM processor. Additionally, he has research interests in high performance compilers (particularly vectorization strategies), dynamic runtimes with a focus on the just-in-time compilation and dynamic execution of code, the C++ language standard, efficient message passing, high performance numerical mathematics libraries and the analysis, modeling and optimization of large-scale parallel scientific or data analytics applications. Prior to joining to Sandia, Simon worked (during his PhD) in a UK Technology Transfer Partnership at the United Kingdom's Atomic Weapons Establishment (AWE).

Clay Hughes is a Senior Member of Technical Staff in the Scalable Computer Architecture group at Sandia National Laboratories. His responsibilities include support for co-design activities using the Structural Simulation Toolkit (SST) and the Heterogeneous Advanced Architecture Platforms. He is heavily involved in the Exascale Computing Project with PathForward and Hardware Technology. His background includes work on a detailed model of hardware transactional memory; development of dynamic power control and run-time scheduling for hardware transactional memory systems; development of a program-less input methodology for binary synthesis to study transactional memory; and



the development of methods to reduce the simulation time for multi-threaded programs. Before joining Sandia, Clay was an Associate Teaching Professor at Florida State University where he supervised three M.S. students, taught undergraduate and graduate courses in computer architecture, ARM and MIPS assembly, real-time systems, and developed new courses in computer system design and embedded systems.

> 4328 Scorpius Street Orlando, FL 32816 WWW.ECE.UCF.EDU