CMOS technology beyond 22nm: Where can silicon take us?

Kelin J. Kuhn
Intel Fellow
Director of Advanced Device Technology
Intel Corporation
Future Challenges in Device Scaling

As near as I can tell: THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

130 nm
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

90 nm
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

65 nm
As near as I can tell: THE key challenge is that the transistors get smaller ...

BUT the *.ppt pictures remain the same size

Future Challenges in Device Scaling
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

32 nm
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

Maybe it would help if we SCALED THEM TOO!

130 nm
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

Maybe it would help if we SCALED THEM TOO!
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

Maybe it would help if we SCALED THEM TOO!
Future Challenges in Device Scaling

As near as I can tell: THE key challenge is that the transistors get smaller …

BUT the *.ppt pictures remain the same size

Maybe it would help if we SCALED THEM TOO!
Future Challenges in Device Scaling

As near as I can tell:
THE key challenge is
that the transistors get
smaller …

BUT the *.ppt pictures
remain the same size

Maybe it would help if we
SCALED THEM TOO!
AGENDA

• Scaling history
• Gate control
  – High-k metal-gate
  – Structural enhancements
• Resistance
• Capacitance
• Mobility
  – Strain
  – Orientation
• Summary
AGENDA

• Scaling history

• Gate control
  – High-k metal-gate
  – Structural enhancements

• Resistance

• Capacitance

• Mobility
  – Strain
  – Orientation

• Summary
MOSFET Scaling

<table>
<thead>
<tr>
<th>Device or Circuit Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimension $t_{ox}, L, W$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Doping concentration $N_a$</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Voltage $V$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Current $I$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Capacitance $\varepsilon A/t$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Delay time/circuit $VC/I$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Power dissipation/circuit $VI$</td>
<td>$1/\kappa^2$</td>
</tr>
<tr>
<td>Power density $VI/A$</td>
<td>$1$</td>
</tr>
</tbody>
</table>

R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling was first described by Dennard in 1974
MOSFET Scaling

<table>
<thead>
<tr>
<th>Device or Circuit Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimension $tox, L, W$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Doping concentration $Na$</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Voltage $V$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Current $I$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Capacitance $\varepsilon A/t$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Delay time/circuit $VC/I$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Power dissipation/circuit $VI$</td>
<td>$1/\kappa^2$</td>
</tr>
<tr>
<td>Power density $VI/A$</td>
<td>$1$</td>
</tr>
</tbody>
</table>

R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling ENDED at the 130nm node (and nobody noticed ...)
90 nm Strained Silicon Transistors

Strained silicon provided increased drive currents, making up for the loss of classical Dennard scaling.
45nm High-k + Metal Gate Transistors

High-k + metal gate transistors restored gate oxide scaling at the 45nm node
Changes in Scaling

**THEN**

- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process

130nm  
90nm  
65nm  
45nm  
32nm
## Changes in Scaling

<table>
<thead>
<tr>
<th>THEN</th>
<th>NOW</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Scaling drove down cost</td>
<td>- Scaling drives down cost</td>
</tr>
<tr>
<td>- Scaling drove performance</td>
<td>- Materials drive performance</td>
</tr>
<tr>
<td>- Performance constrained</td>
<td>- Power constrained</td>
</tr>
<tr>
<td>- Active power dominates</td>
<td>- Standby power dominates</td>
</tr>
<tr>
<td>- Independent design-process</td>
<td>- Collaborative design-process</td>
</tr>
</tbody>
</table>
MOSFET Challenges

- Resistance (Decreased S/D opening)
- Capacitance (Increased fringe to contact/facet)
- Gate control (SCE limitations with smaller Leff)
- Mobility (Reduced strain with decreased pitch)
MOSFET Challenges

- Resistance (Decreased S/D opening)
- Capacitance (Increased fringe to contact/facet)
- Gate control (SCE limitations with smaller Leff)
- HiK Metal Gate
- Mobility (Reduced strain with decreased pitch)
High-k Metal Gate

**BENEFITS**

- **High-k gate dielectric**
  - Reduced gate leakage
  - Continued $T_{OX}$ scaling

- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolve $V_T$ pinning for poly on high-k gate dielectrics

**CHALLENGES**

- **High-k gate dielectric**
  - Reduced reliability
  - Reduced mobility

- **Metal gates**
  - Dual bandedge workfunctions
  - Thermal stability
  - Process integration

K. Mistry - IEDM 2007
High-k/MG enables 0.7X ToxE scaling while reducing Ig >> 25X for NMOS and 1000X for PMOS.

23% better than 65 nm at the same leakage and 100mV lower Vcc. (FO=2 delay of 5.1 ps at $I_{OFFN} = I_{OFFP} = 100\ \text{nA}/\mu\text{m}$)

K. Mistry - IEDM 2007
FOUR GENERATION COMPARISON

45nm:
1st gen. HiK-MG
Mistry, Intel, IEDM 2007

32nm:
2nd gen. HiK-MG
Natarajan, Intel, IEDM 2008
MOSFET Challenges

- Resistance (Decreased S/D opening)
- Capacitance (Increased fringe to contact/facet)
- Gate control (SCE limitations with smaller Leff)
- Mobility (Reduced strain with decreased pitch)
- New architectures

Gate control (SCE limitations with smaller Leff)
Ultra-thin body with RSD
Ultra-thin body with RSD

- Raised source drain (RSD)
- Ultra-thin body (UTB)
MuGFET

Vertical thin body
MuGFET with RSD

Vertical thin body with raised S/D (RSD) architecture
Nanowire with RSD

Nanowire with raised S/D (RSD) architecture
Looking at all these in more detail
Ultra-thin body with RSD

Benefits

- Extension of planar technology (less disruptive to manufacturing)
- Improved RDF (low doped channel)
- Excellent channel control
- Potential for body bias

Compatible with RSD technology
Ultra-thin body with RSD

Challenges

- Capacitance: (Increased fringe to contact/facet)
- Variation: (film thickness changes affects VT and DIBL)
- Strain: (strain transfer from S/D into the channel)
- Performance: (transport challenges with thin Tsi)
- Manufacturing: (requires both thin Tsi and thin BOX)
- Rext: (Xj/Tsi limitations)
- Variation: (film thickness changes affects VT and DIBL)
- Strain: (strain transfer from S/D into the channel)
- Performance: (transport challenges with thin Tsi)
- Manufacturing: (requires both thin Tsi and thin BOX)
Ultra-thin body

Barral – CEA-LETI – IEDM 2007

Cheng – IBM – VLSI 2009

NFET
Silicide
Faceted epi

PFET

20nm

Ultra-thin body

Drain current $I_{DS}$ (A/μm)

Gate voltage $V_{GS}$ (V)

$V_{DS} = 1V$

$W = 10μm$

$n$-sSOI
$I_{ON} = 350μA/μm$
$I_{OFF} = 10^{-7}A/μm$

$p$-sSOI
$I_{ON} = 170μA/μm$
$I_{OFF} = 10^{-11}A/μm$

$n$-SOI
$I_{ON} = 780μA/μm$
$I_{OFF} = 10^{-7}A/μm$

$p$-SOI
$I_{ON} = 230μA/μm$
$I_{OFF} = 10^{-11}A/μm$

Si film thickness $t_{Si}$ (nm)

DIBL (mV/µm)

$V_{SS} = 0.9 V$

$V_{SS} = 0.05 V$

$L_g = 25nm$

$T_{Si} = 6nm$

$DIBL = 85 mV/µm$

$DIBL = 90 mV/µm$

SS = 80 mV/dec

SS = 85 mV/dec

Intel

Kelin Kuhn / CNNA / Berkeley / 2010
MuGFET

Benefits

- Double-gate relaxes Tsi requirements
  - Fin Wsi > UTB Tsi
  - (less scattering, improved VT shift)

- Nearly ideal sub-threshold slope
  - (gates tied together)

- Improved RDF
  - (low doped channel)

- Excellent channel control

- Can be on bulk or SOI
MuGFET with RSD

**Benefits**

- Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)
- Nearly ideal sub-threshold slope (gates tied together)
- Improved RDF (low doped channel)
- Excellent channel control
- Compatible with RSD technology
- Nearly ideal sub-threshold slope (gates tied together)
MuGFET

Benefits

Double-gate relaxes Tsi requirements
Fin Wsi > UTB Tsi
(less scattering, improved VT shift)

Possibility for independent gate operation

Improved RDF
(low doped channel)

Excellent channel control
MuGFET

Challenges

- Capacitance (fringe to contact/facet)
  Plus, additional “dead space” elements

- Small fin pitch
  (2 generation scale?)

- Fin Strain engr.
  (Effective strain transfer from a fin into the channel)

- Variation
  (Mitigating RDF but acquiring Hsi/Wsi/epi)

- Gate wraparounds
  (Endcap coverage)

- Fin/gate fidelity on 3’D
  (Patterning/etch)

- Topology
  (Polish / etch challenges)

- Rext:
  (Xj/Wsi limitations)

- Variation
  (Mitigating RDF but acquiring Hsi/Wsi/epi)

A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi†,
Kazuya Asano**, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*
Central Research Laboratory, Hitachi Ltd., *) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.

1. Folded channel MOSFET layout design and device structure.
   bottom is A-A cross section, and the right is B-B cross section
Kavalieros – Intel – IEDM 2006

Vellianitis – NXP-TSMC – IEDM 2007
MuGFET

Kang – Sematech – VLSI 2008

Chang – TSMC – IEDM 2009
Nanowire further relaxes $T_{Si}$ / $W_{Si}$ requirements.

Nearly ideal sub-threshold slope (gates tied together).

Improved RDF (low doped channel).

Excellent channel control.
Nanowire

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Compatible with RSD technology
- Improved RDF (low doped channel)
- Excellent channel control
Nanowire further relaxes Tsi / Wsi requirements

Possibility for independent gate operation

Improved RDF (low doped channel)

Excellent channel control

Nanowire Benefits
Nanowire

Challenges

- Gate conformality (dielectric and metal)
- Capacitance (fringe to contact/facet)
  Plus, additional “dead space” elements
- Variation (Mitigating RDF but acquiring a myriad of new sources)
- Fin/gate fidelity on 3’D (Patterning/etch)
- Topology (Polish / etch challenges)
- Integrated wire fabrication (Epitaxy? Other?)
- Wire stability (bending/warping)
- Mobility degradation (scattering)
- Fin Strain engr. (Effective strain transfer from wire into the channel)
- Rext: (Xj/Wsi limitations)
- Capacitance (fringe to contact/facet)
  Plus, additional “dead space” elements
- Variation (Mitigating RDF but acquiring a myriad of new sources)
- Fin/gate fidelity on 3’D (Patterning/etch)
- Topology (Polish / etch challenges)
- Integrated wire fabrication (Epitaxy? Other?)
- Wire stability (bending/warping)
- Mobility degradation (scattering)
- Fin Strain engr. (Effective strain transfer from wire into the channel)
- Rext: (Xj/Wsi limitations)
Nanowire FETs

Yeo – Samsung – IEDM 2006

(a) 3D-NWFET

(b) ΦFET

Dupre – CEA-LETI – IEDM 2008
Nanowire FETs

Wong – NUS Singapore – VLSI 2009

Bangsaruntip – IBM – IEDM 2009
Challenges for ALL Architectures

Resistance
Capacitance
Mobility
Planar Resistive Elements

- $R_{\text{CONTACT}}$
- $R_{\text{SILICIDE}}$
- $R_{\text{INTERFACE}}$
- $R_{\text{EPI}}$
- $R_{\text{SPREADING}}$
- $R_{\text{ACCUMULATION}}$
Improvement in Planar Elements

- Evolutionary $R_{\text{acc}}$ improvement through $X_j$ scaling (anneal/implant) until the end of the planar roadmap (thereafter Tsi/Wsi limited)
- $R_{\text{epi}} / R_{\text{spreading}}$ improvement from raised source/drain (RSD)
- Limited $R_{\text{silicide}}$ improvement (NiSi has the lowest known resistivity)
- Significant possibility for $R_{\text{interface}}$ improvement, particularly through SBH optimization ($R_{\text{interface}}$).
- $R_{\text{contact}}$ improvement from high conductivity metals (copper?)

$R_{\text{interface}} \propto \exp \left( \frac{q \phi_B}{\sqrt{N_D}} \right)$

$q \phi_B$ – Schottky Barrier Height (SBH)
$N_D$ – Substrate doping concentration
$A$ – Contact area
Improvement in Planar Elements

- Evolutionary $R_{\text{acc}}$ improvement through $X_j$ scaling (anneal/implant) until the end of the planar roadmap (thereafter Tsi/Wsi limited)
- $R_{\text{epi}} / R_{\text{spreading}}$ improvement from raised source/drain (RSD)
- Limited $R_{\text{silicide}}$ improvement (NiSi has the lowest known resistivity)
- Significant possibility for $R_{\text{interface}}$ improvement, particularly through SBH optimization ($R_{\text{interface}}$).
- $R_{\text{contact}}$ improvement from high conductivity metals (copper?)

```
\begin{equation}
R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)
\end{equation}
```

$q\phi_B$ – Schottky Barrier Height (SBH)

$N_D$ – Substrate doping conc.

$A$ – Contact area
Schottky theory vs. experimental SBHs for metals on nSi
Mukherjee – Intel

Fermi level pinned to mid-gap for most metals on Si

K. Kuhn – IEDM SC 2008

Kelin Kuhn / CNNA / Berkeley / 2010
Alloy and Implant Modifications to Silicides

Lee – NUS-Singapore
IEDM 2006
Ni-alloy silicides

Zhang – KTH Sweden
EDL 2007
Implant modification of SBH
(SB FET paper)
Schottky barrier S/D – an option?

- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height $\phi_b$.
- The extreme limit for metal in the S/D regions (with associated improvements in $R_{ext}$)
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)
Metal S/D Id-Vg Characteristics (Zhu)

- Two possible conduction paths:
  - Thermionic – over the barrier – good subthreshold slope
  - Tunneling – through the barrier – poor subthreshold slope

- Two options to achieve thermionic control
  - Very low Schottky barrier height (<100meV)
  - Very heavy doping close to the barrier -> form thin doped s/d
Metal S/D – Benefits/Challenges

Benefits

• Low bulk resistance contacts to the channel
• Very abrupt junctions, allowing precise overlap/underlap
• No random s/d dopant fluctuation effects
• Minimize possible s/d carrier-carrier scattering effects with the channel

Challenges

• Poor experimental drive currents
• Requires very low Schottky barriers, low resistance interfaces
• Ambipolar conduction (high drain-body leakage for bulk devices)
• Early contact formation limits midsection process temperatures
• Need alternative approach for s/d stressors
Challenges for ALL Architectures

Resistance
Capacitance
Mobility
Planar Capacitive Elements

- Cfringe to contact
- Cfringe to facet
- Cfringe to diffusion (of/ff)
- Cxud - device component of Cov (XUD-based)
- Channel component of Cgate
- Area junction
- Gated-edge junction
- Junction

Kuhn, Intel, IEDM SC 2008
Planar Capacitive Elements

“Golden” days of scaling: Who worried about Cfringe?
Planar Capacitive Elements

“Silver” days of scaling: Introduction of epi: Increased fringe due to facet
Planar Capacitive Elements

“Bronze” days of scaling
Gate and contact CD dimensions scaling slower than contacted gate pitch – fringe matters
Innovative Spacer Technologies

SPACER REMOVAL
Liow – NUS Singapore
EDL 2008

SiBCN (Low-K) SPACER
Ko – TSMC
VLSI 2008
Challenges for ALL Architectures

Resistance

Capacitance

Mobility

Challenges for ALL Architectures
Transistor Performance Trend

Strain is a critical ingredient in modern transistor scaling. Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation.
Etch-stop nitride (CESL)

- **Ito – NEC**
  - IEDM 2000
  - NMOS SiN strain

- **Pidin – Fujitsu**
  - IEDM 2004
  - N and PMOS

- **Mayuzumi – Sony**
  - IEDM 2007
  - Dual-cut stress liners (MG process)
Strain: Pitch dependence

NMOS
Pitch degradation increases with film pinchoff, requires higher stress, thinner films

PMOS
eSiGe S/D mobility strongly dependent on pitch

Auth, Intel, VLSI 2008
Embedded SiGe (PMOS)

Thompson – Intel
IEDM 2002 / 2004

Ghani – Intel
IEDM 2003

Chidambaram
TI / Applied Materials
VLSI - 2004
Embedded Si:C (NMOS)

Ang – NUS-Singapore
IEDM 2004
Selective epi SiC (undoped)

Yang – IBM
IEDM 2008
In-situ epi P-SiC

Chung – Nat’l Chiao Tung U.
VLSI 2009
Implanted C + SPE

Kelin Kuhn / CNNA / Berkeley / 2010
Strain: Pitch dependence

NMOS Pitch degradation increases with film pinchoff, requires higher stress, thinner films

PMOS eSiGe S/D mobility strongly dependent on pitch

Auth, Intel, VLSI 2008
### Strain: Pitch dependence

What about strain options less sensitive to pitch?
Stress Memorization (SMT)

Ota – Mitsubishi
IEDM 2002
NMOS SMT

Chen – TSMC
VLSI 2004
NMOS SMT

Wei – AMD
VLSI 2007
Multiple liners
Metal stress (gate and contact)

Different gate stack

Raised S/D

NMOS

PMOS

5.4-6.5%

Kang – Sematech
IEDM 2006

Auth – Intel
VLSI 2008

Kelin Kuhn / CNNA / Berkeley / 2010
Enhanced PMOS strain: Gate last HiK-MG

Before gate removal  After gate removal


14% RMG

VDD = 1.0V
65nm [Tyagi, 2005 IEDM]
(100) surface – top down

- Standard wafer / direction
- (100) Surface / <110> channel
- (100) Surface / <100>
- (a “45 degree” wafer)

Both <110> directions are the same.

(110) surface – top down

- Non-standard
- (110) Surface
- Three possible channel directions
- <110> <111> and <100>
(100) surface – top down

Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.

(110) surface – top down

Non-standard
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS

(110) <110> BEST PMOS

Electron mobility on (110) vs. (100)

Hole mobility on (110) vs. (100)

Yang
AMD/IBM
EDST 2007
(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

PMOS Vertical Devices on (100)

Chang - IBM – TED 2004

Kinugawa-Toshiba VLSI 1986
(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography
Wafer bonding; SOI of opposite type of handle wafer; both options (N and PMOS SOI explored)

Early HOT

Elegant solution!

Yang – IBM
IEDM 2003 [28]
First HOT

Yang – AMD/IBM
VLSI 2004
HOT RO

V_{dd} = 1.2V
W_{n} = 4μm
W_{p} = 6μm
t_{ox} = 2.2nm

Delay (ps/stage)

I_{offN + I_{offP}} (A)

21%
Strain AND orientation optimization

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Longitudinal</td>
<td>X  Tensile</td>
<td>Compressive</td>
</tr>
<tr>
<td>Lateral</td>
<td>Y  Tensile</td>
<td>Tensile</td>
</tr>
<tr>
<td>Si Depth</td>
<td>Z  Compressive</td>
<td>Tensile</td>
</tr>
</tbody>
</table>

Chan – IBM
CICC 2005

Krishnamohan – Stanford
IEDM 2008
More complex for non-(100) orientations

(100) Surface (k⊥=0)  (001) Surface (k⊥=0)  (001) Surface Vg=-1V

(100) Surface Vg=-1V, Sxx=-1GPa

(110) Surface (k⊥=0)  (110) Surface Vg=-1V  (110) Surface Vg=-1V, Sxx=-1GPa

BULK  1’D CONFINED  1’D CONFINED STRAINED

Kuhn/Packan, Intel, IEDM 2008  Klein Kuhn / CNNA / Berkeley / 2010
AGENDA

• Scaling history
• Gate control
  – High-k metal-gate
  – Structural enhancements
• Resistance
• Capacitance
• Mobility
  – Strain
  – Orientation

• Summary
Looking Forward

<table>
<thead>
<tr>
<th>Low risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Further enhancements in strain technology</td>
</tr>
<tr>
<td>Further enhancements in HiK-MG technology</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Medium Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimized substrate and channel orientation</td>
</tr>
<tr>
<td>Reduction in MOS parasitic resistance</td>
</tr>
<tr>
<td>Reduction in MOS parasitic capacitance</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>High risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>UTB devices</td>
</tr>
<tr>
<td>MuGFETS</td>
</tr>
<tr>
<td>Nanowires</td>
</tr>
<tr>
<td>Metal S/D devices</td>
</tr>
</tbody>
</table>
Questions???