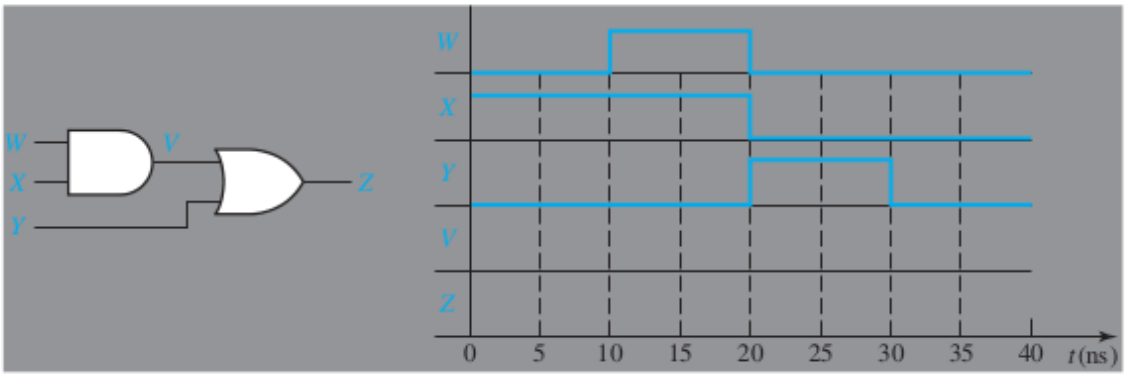
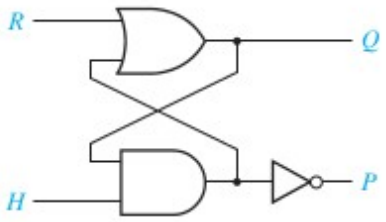
8.1 Complete the timing diagram for the given circuit. Assume that both gates have a propagation delay of 5 ns.



9.15 Show how to make a 4-to-1 MUX, using an 8-to-1 MUX.

9.16 Implement a 32-to-1 multiplexer using two 16-to-1 multiplexers and a 2-to-1 multiplexer in two ways: (a) Connect the most significant select line to the 2-to-1 multiplexer, and (b) connect the least significant select line to the 2-to-1 multiplexer.

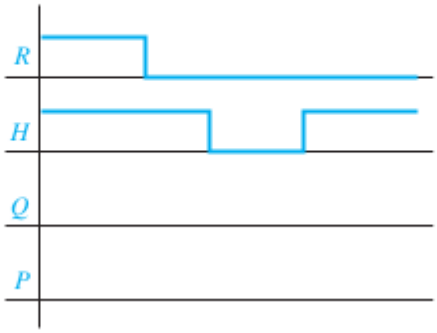
11.2 A latch can be constructed from an OR gate, an AND gate, and an inverter connected as follows:



(a) What restriction must be placed on R and H so that P will always equal Q' (under steady-state conditions)?

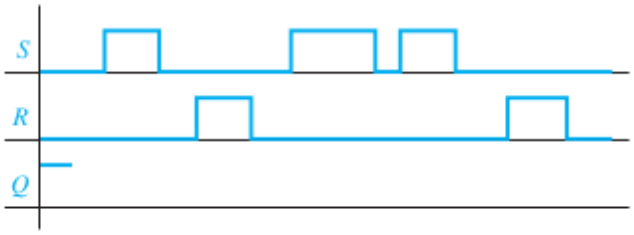
(b) Construct a next-state table and derive the characteristic (next-state) equation for the latch.

(c) Complete the following timing diagram for the latch.

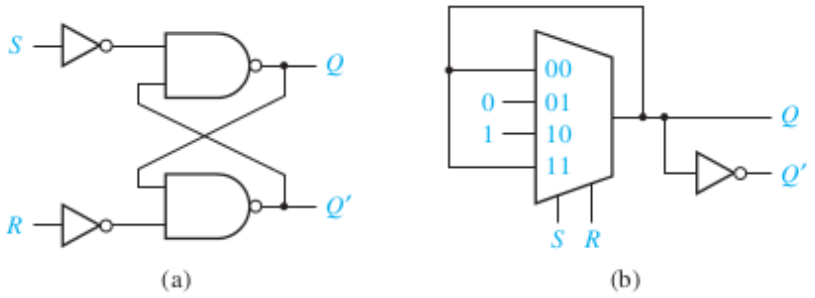


11.10 Convert by adding external gates:
(a) a D flip-flop to a J-K flip-flop.
(b) a T flip-flop to a D flip-flop.
(c) a T flip-flop to a D flip-flop with clock enable.

11.11 Complete the following timing diagram for an S-R latch. Assume Q begins at 1.



11.12 Using a truth table similar to Figure 11-8(b), confirm that each of these circuits is an S-R latch. What happens when $S = R = 1$ for each circuit?



11.14 (a) Construct a state table for this circuit and identify the stable states of the circuit.
(b) Derive a Boolean algebra equation for the next value of the output Q in terms of Q, A and B.
(c) Analyze the behavior of the circuit. Is it a useful circuit? If not, explain why not; if yes, explain what it does.