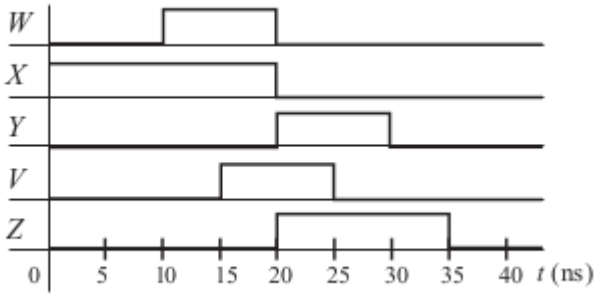
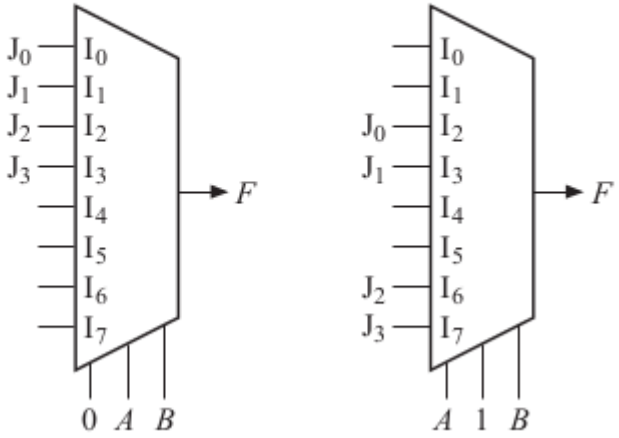
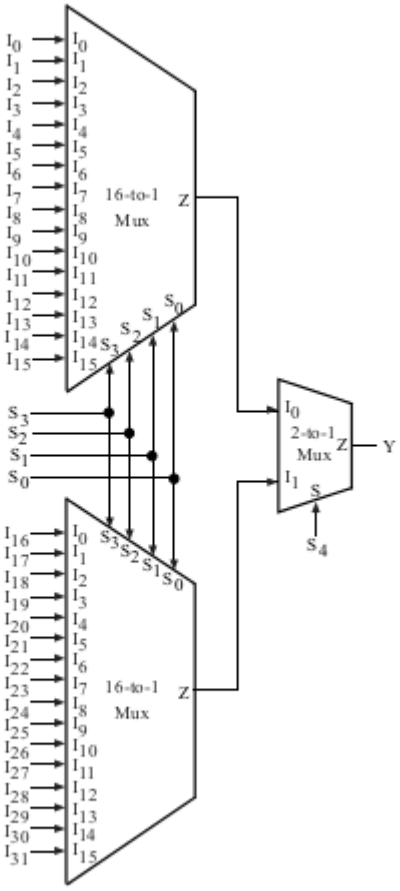
8.1



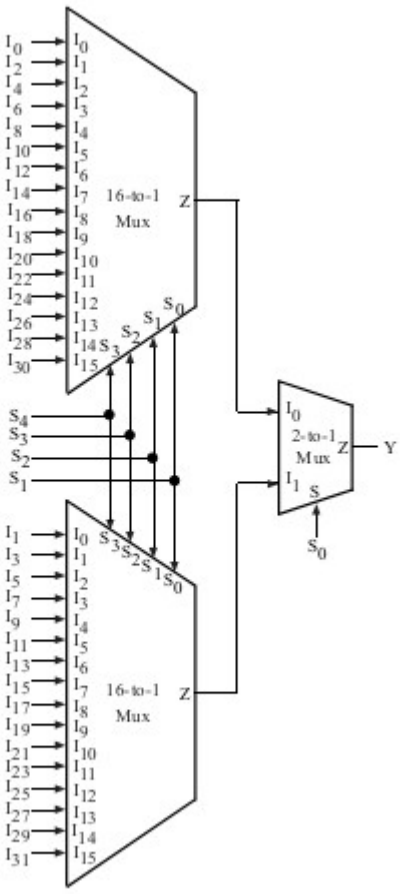
9.15 There are many solutions. For example:



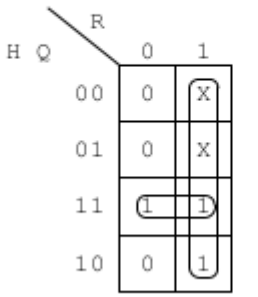
9.16



9.16 contd



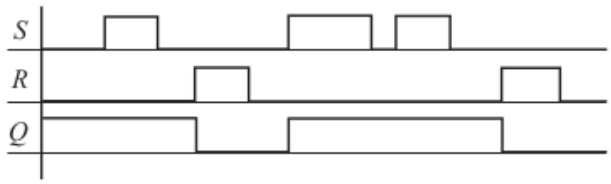
11.2 See FLD p. 713 for solution. For part (b), also use the following Karnaugh map. Don't cares come from the restriction in part (a).



$Q^+ = R + HQ$

11.10 See FLD p. 715 for solution.

11.11



11.12 For every input/state combination with the condition $SR = 0$ holding, each circuit obeys the next-state equation $Q^+ = S + R'Q$. When $S = R = 1$, in (a), both outputs are 1, and in (b), the latch holds its state.

11.14 (a)

Present State Q	Next State Q^+ A B			
	00	01	11	10
0	**0**	**0**	**0**	1
1	0	0	**1**	**1**

11.14 (b) & (c) $Q^+ = A(B' + Q)$
This is a reset dominant latch where A' acts a reset and B' acts as a set.