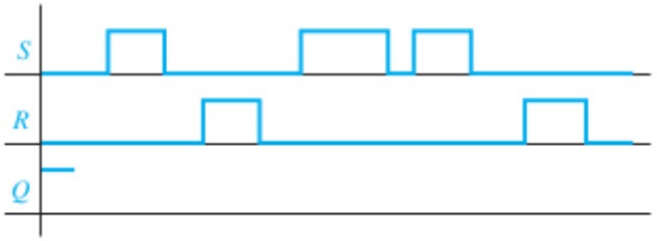
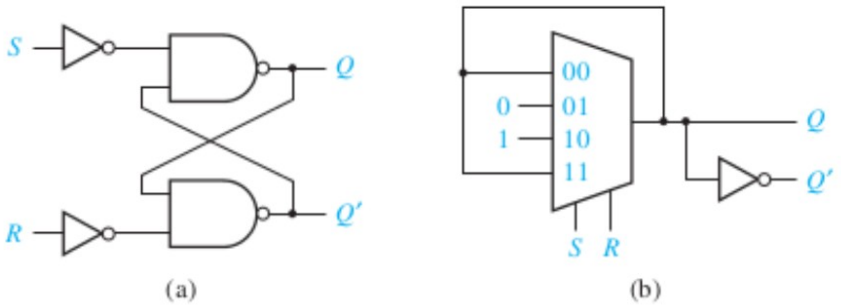
11.10 Convert by adding external gates:
(a) a D flip-flop to a J-K flip-flop.
(b) a T flip-flop to a D flip-flop.
(c) a T flip-flop to a D flip-flop with clock enable.

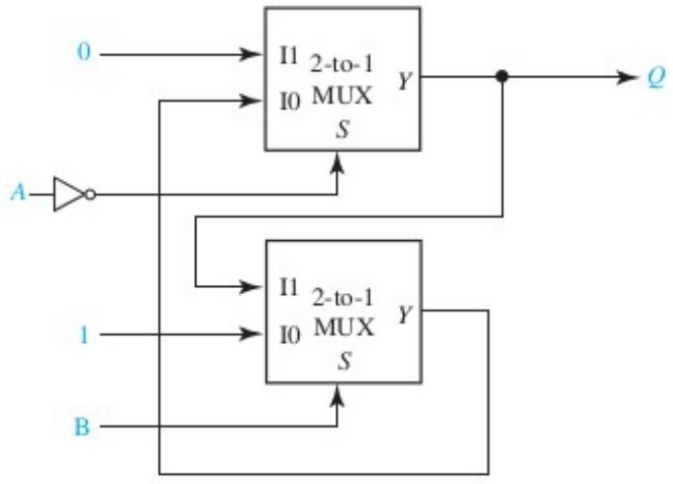
11.11 Complete the following timing diagram for an S-R latch. Assume Q begins at 1.



11.12 Using a truth table similar to Figure 11-8(b), confirm that each of these circuits is an S-R latch. What happens when $S = R = 1$ for each circuit?



11.14 (a) Construct a state table for this circuit and identify the stable states of the circuit.
(b) Derive a Boolean algebra equation for the next value of the output Q in terms of Q, A and B.
(c) Analyze the behavior of the circuit. Is it a useful circuit? If not, explain why not; if yes, explain what it does.



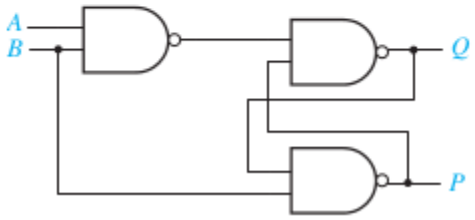
11.16 Analyze the latch circuit shown.

(a) Derive the next-state equation for this circuit using Q as the state variable and P as an output.

(b) Construct the state table and output table for the circuit. Circle the stable states of the circuit.

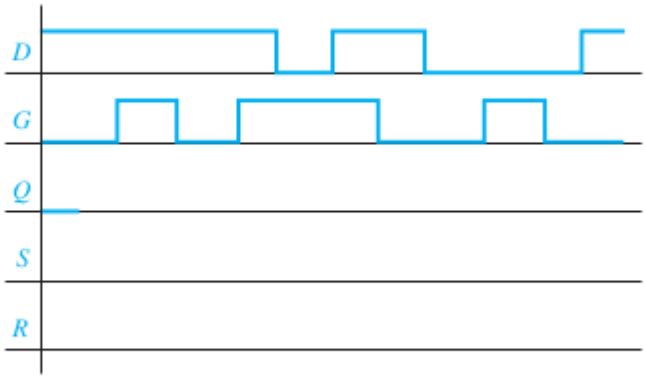
(c) Are there any restrictions on the allowable input combinations on A and B? Explain your answer.

(d) Is the output P usable as the complement of Q? Verify your answer.



11.18 Complete the following timing diagrams for a gated D latch. Assume Q begins at 0.

(a) First draw Q based on your understanding of the behavior of a gated D latch.



(b) Now draw in the internal signals S and R from Figure 11-11, and confirm that S and R give the same value for Q as in (a).

11.27 (a) Construct a D flip-flop using an inverter and an S-R flip-flop.

(b) If the propagation delay and setup time of the S-R flip-flop in (a) are 2.5 ns and 1.5 ns, respectively, and if the inverter has a propagation delay of 1 ns, what are the propagation delay and setup time of the D flip-flop of Part (a)?

12.6 Design a circuit using D flip-flops that will generate the sequence 0, 0, 1, 0, 1, 1 and repeat. Do this by designing a counter for any sequence of states such that the first flip-flop takes on this sequence. There are many correct answers, but do not duplicate states, because each state can have only one next state.

12.7 Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . .
(a) Use D flip-flops
(b) Use T flip-flops
In each case, what will happen if the counter is started in state 000?

12.8 Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . .
(a) Use J-K flip-flops
(b) Use S-R flip-flops
In each case, what will happen if the counter is started in state 000?

12.19 Design a 3-bit counter which counts in the sequence:
001, 100, 101, 111, 110, 010, 011, 001, . . .
(a) Use D flip-flops.
(b) Use J-K flip-flops.
(c) Use T flip-flops.