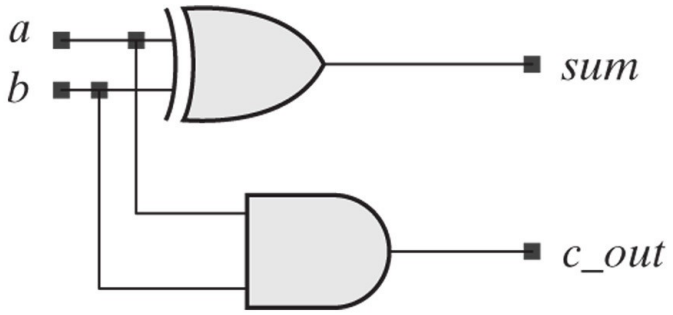
EEL 4783: HDL in Digital System Design

Lecture 2: Introduction to Logic Design with Verilog

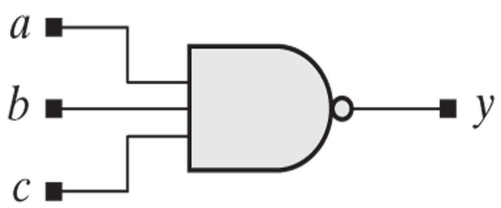
Prof. Mingjie Lin

Schematic and Verilog description of a half adder.

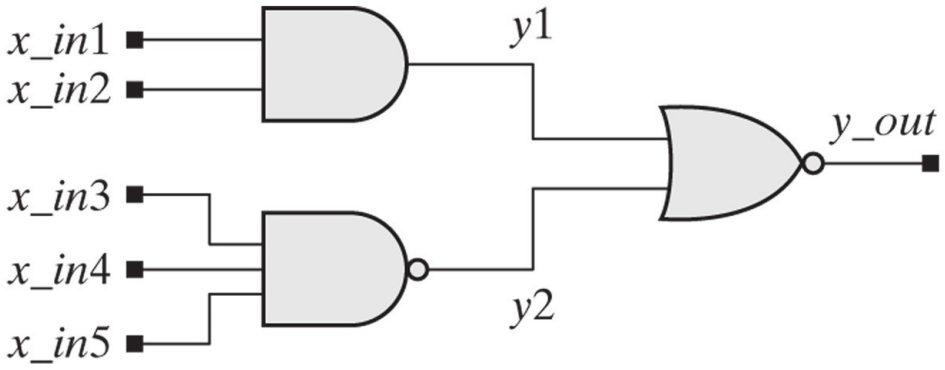



```
module Add_half (output c_out, sum, input a, b);
   xor    (sum, a, b);
   and    (c_out, a, b);
endmodule
```

Examples




```
...
nand (y, a, b, c);
...
```




```
wire    y1, y2;
nor     (y_out, y1, y2);
and     (y1, x_in1, x_in2);
nand    (y2, x_in3, x_in4, x_in5);
```

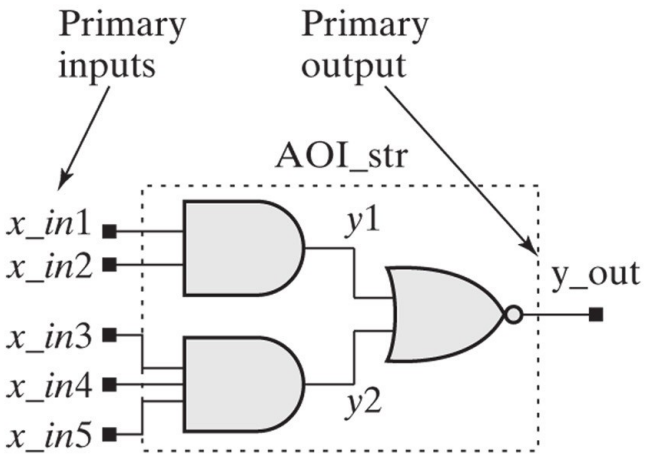
TABLE 4-1 Verilog primitives for modeling combinational logic gates.

n-Input	*n*-Output, 3-state
and	buf
nand	not
or	bufif0
nor	bufif1
xor	notif0
xnor	notif1

The format of a Verilog module

```
module my_design (module_ports);
...  // Declarations of ports go here
...  // Functional details go here
endmodule
```

An AOI Circuit



Module name

Module ports

```
module AOI_str_1995 (y_out, x_in1, x_in2, x_in3, x_in4, x_in5);
  output y_out;
  input  x_in1, x_in2, x_in3, x_in4, x_in5;

  wire   y1, y2;

  nor    (y_out, y1, y2);
  and    (y1, x_in1, x_in2);
  and    (y2, x_in3, x_in4, x_in5);
endmodule
```

Port modes

Internal wires establish connectivity

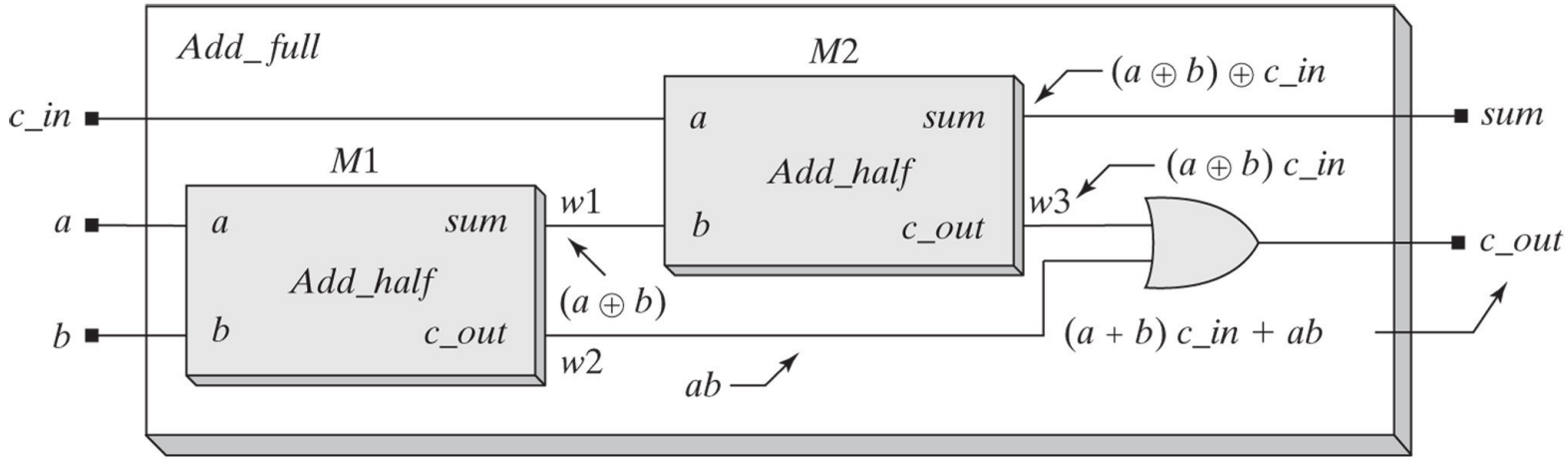
Instantiated primitives

(a)

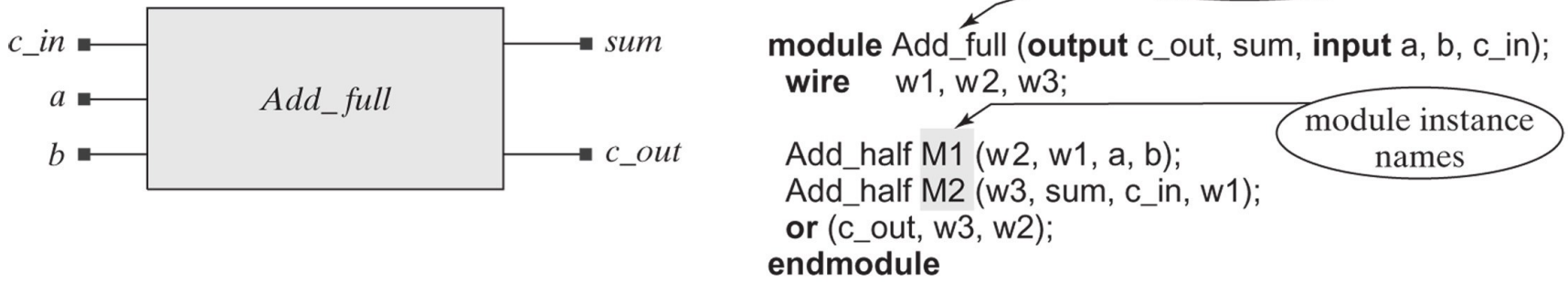
```
module AOI_str_2005 (output y_out, input x_in1, x_in2, x_in3, x_in4, x_in5);
 wire    y1, y2;

 nor     (y_out, y1, y2);
 and     (y1, x_in1, x_in2);
 and     (y2, x_in3, x_in4, x_in5);
endmodule
```

(b)

Hierarchical decomposition of a full adder: (a) gate-level schematic and (b) Verilog model

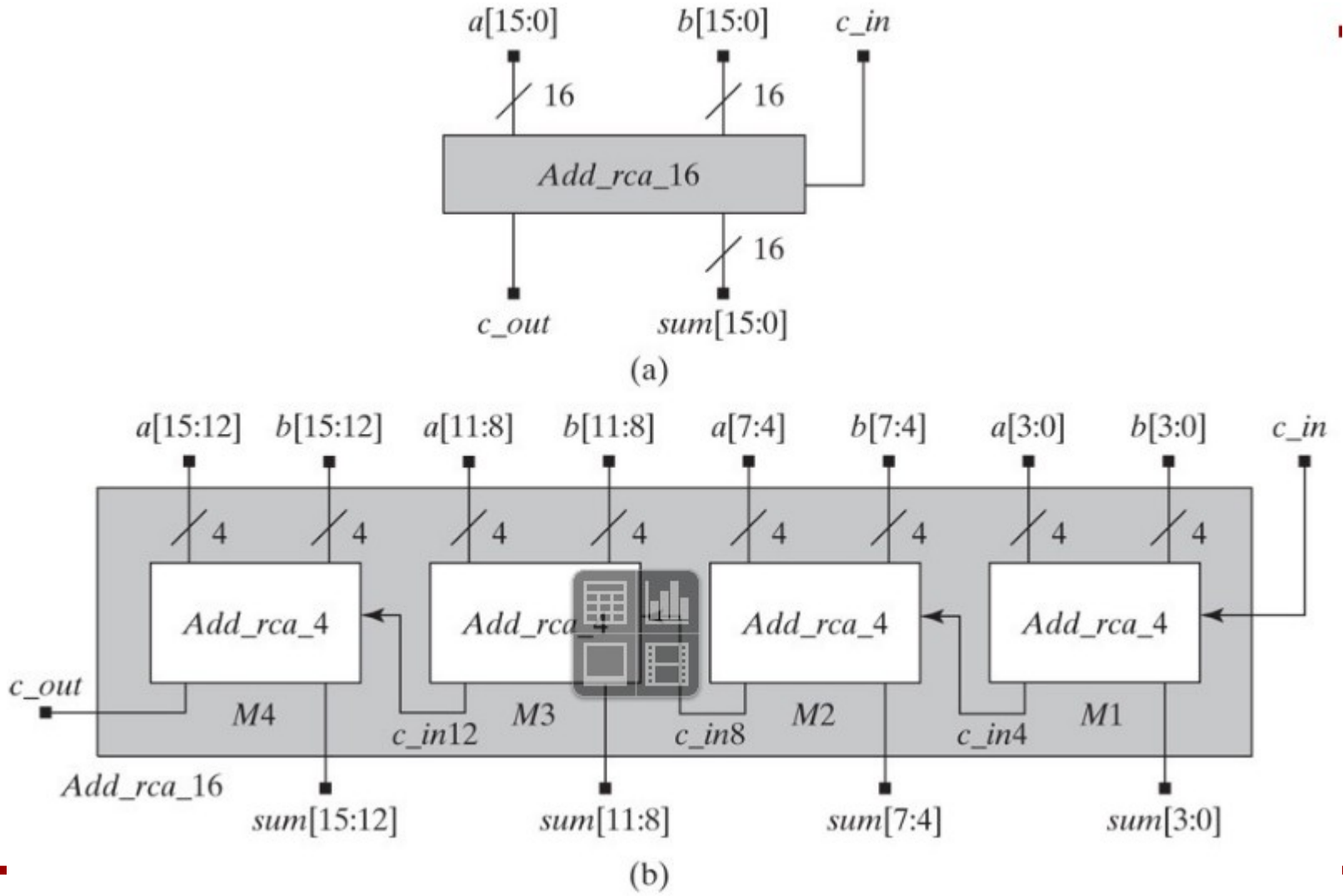


(a)

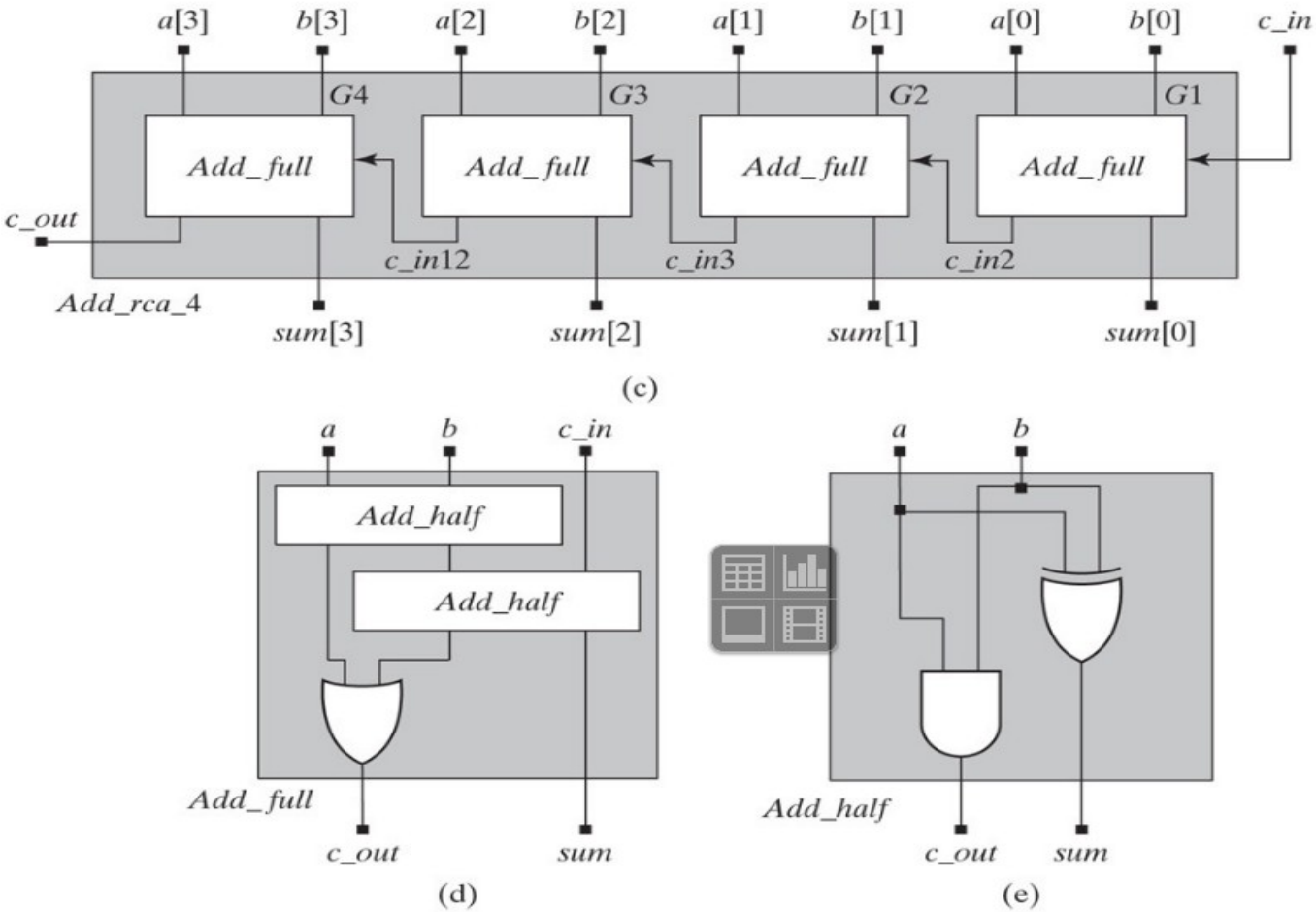


(b)

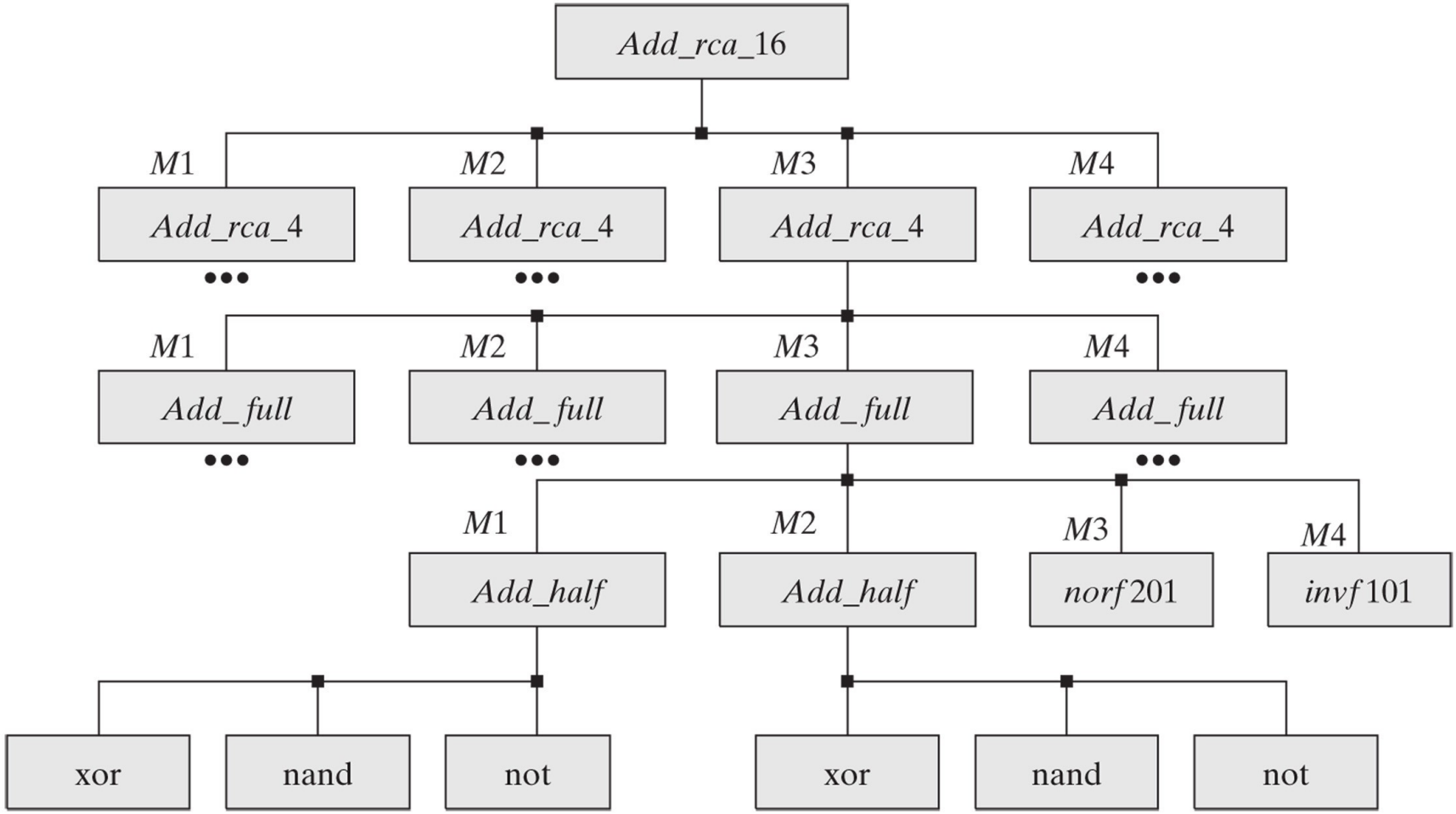
Hierarchical decomposition of a 16-bit, ripple-carry adder



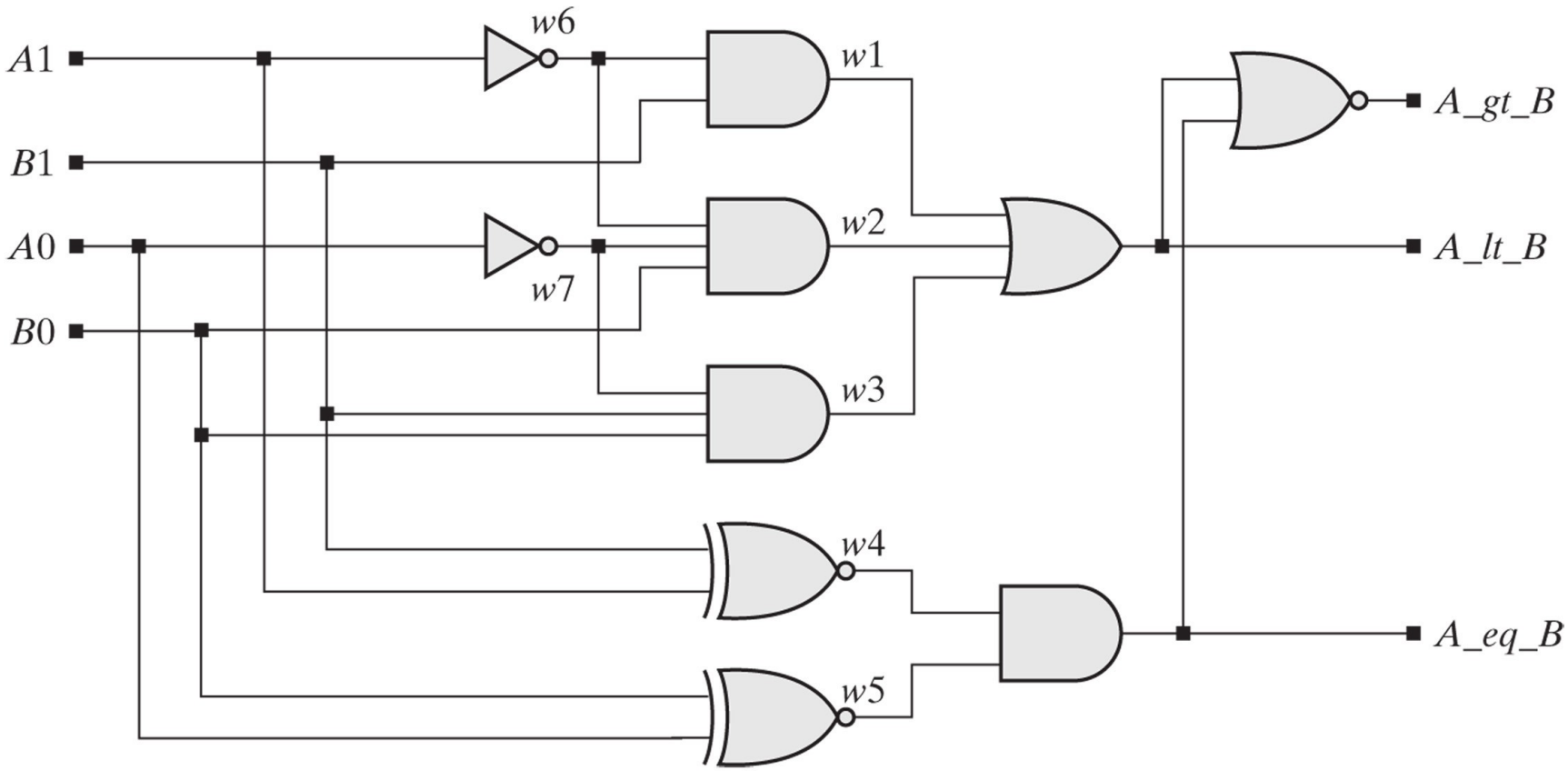
Hierarchical decomposition of a 16-bit, ripple-carry adder (cont.)



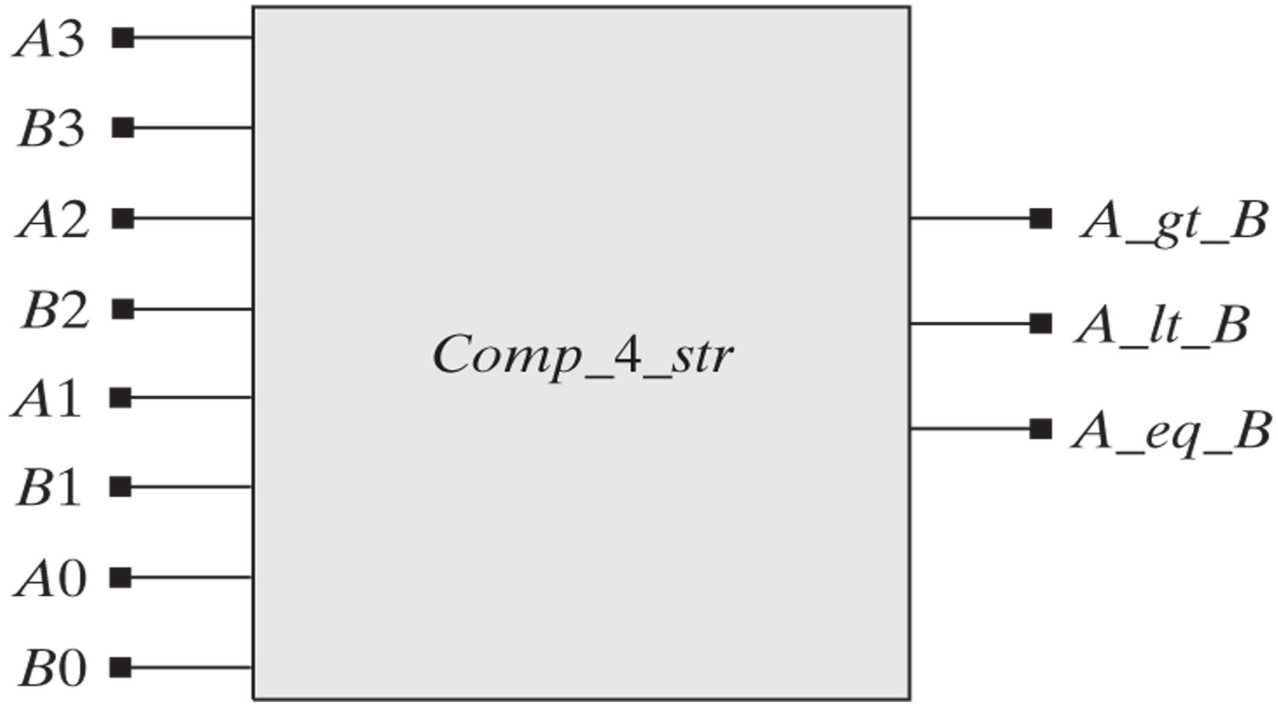
Design hierarchy of a 16-bit ripple-carry adder.



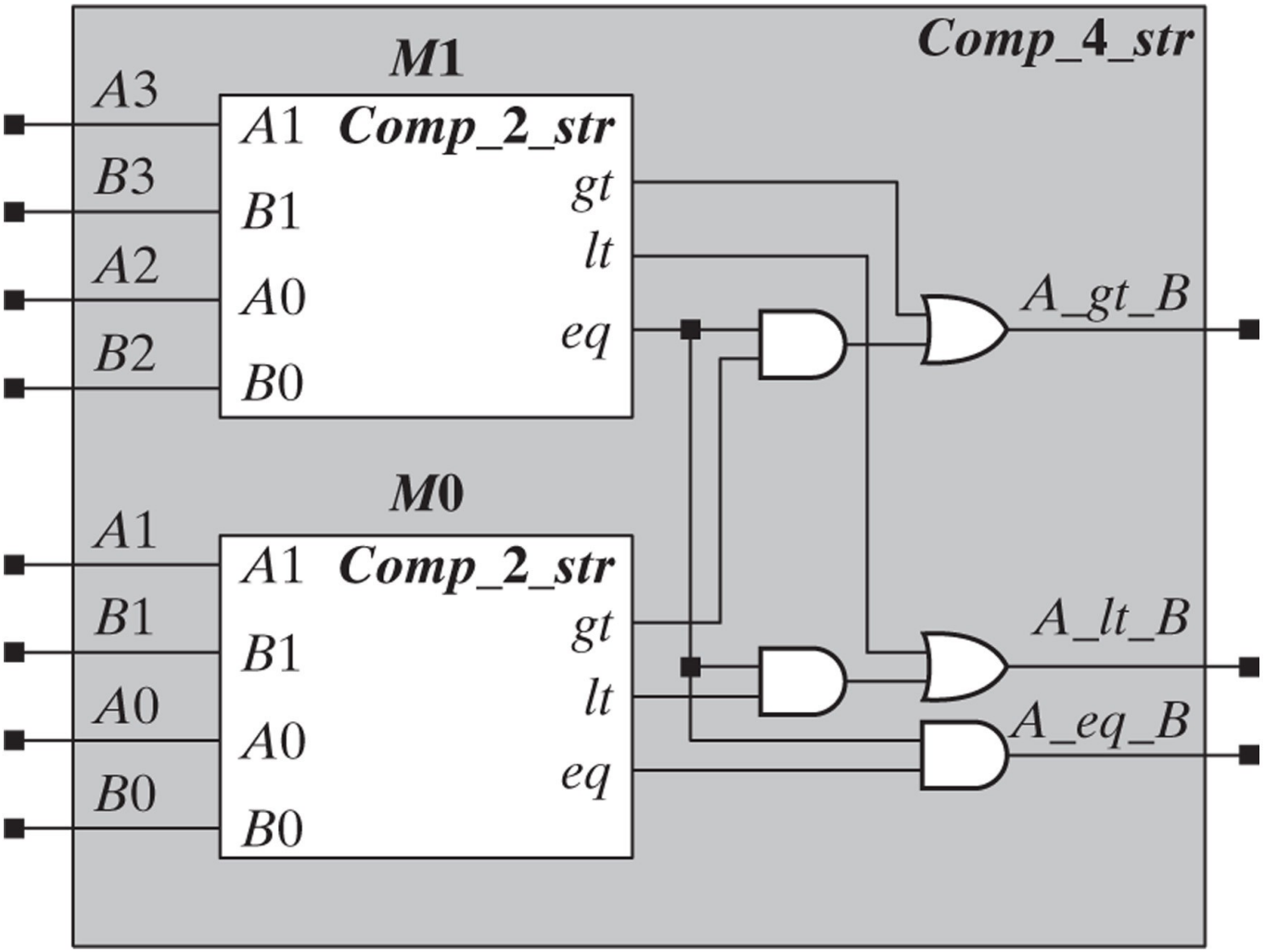
Schematic of a 2-bit binary comparator.



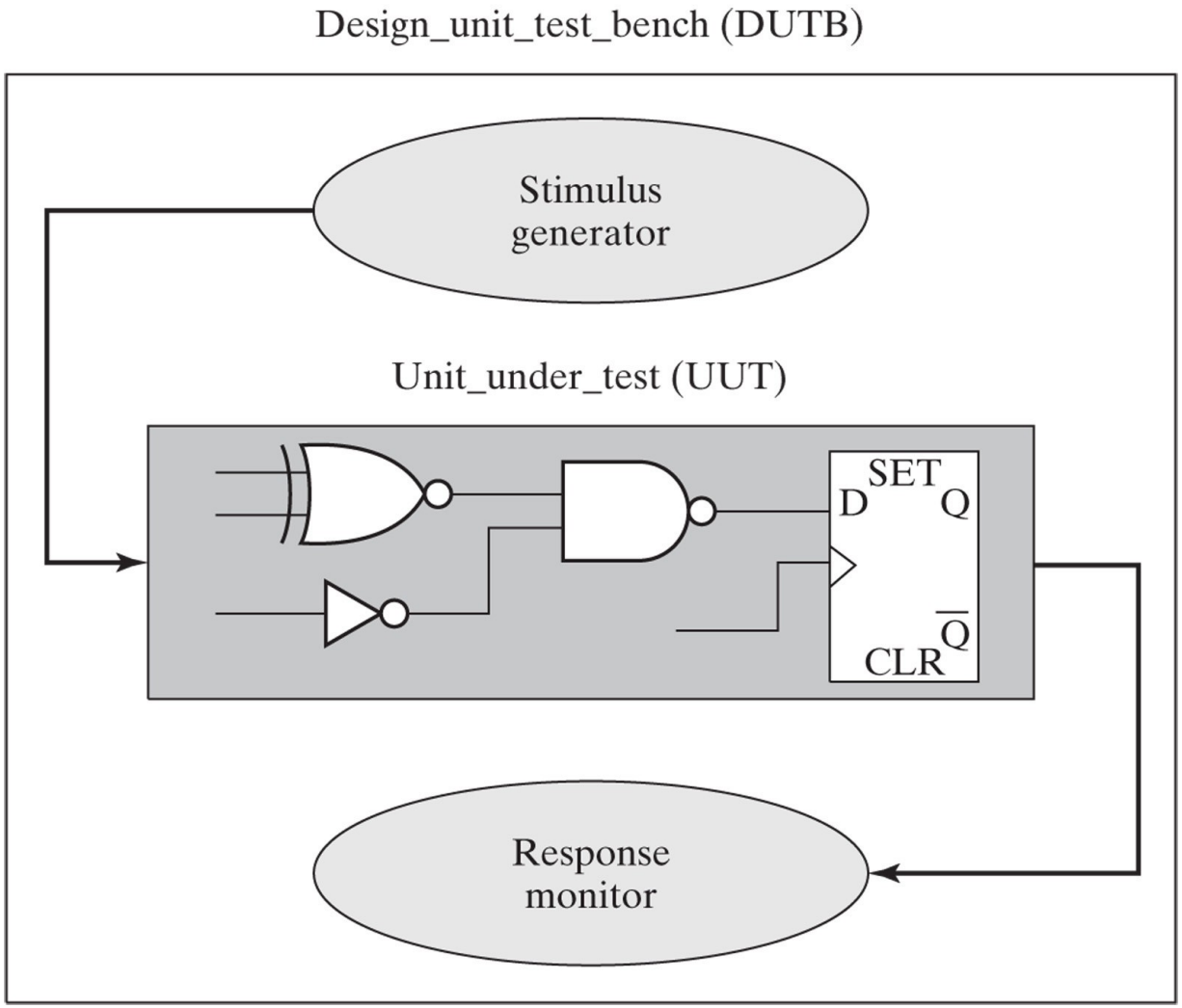
Block diagram symbol of a 4-bit comparator.



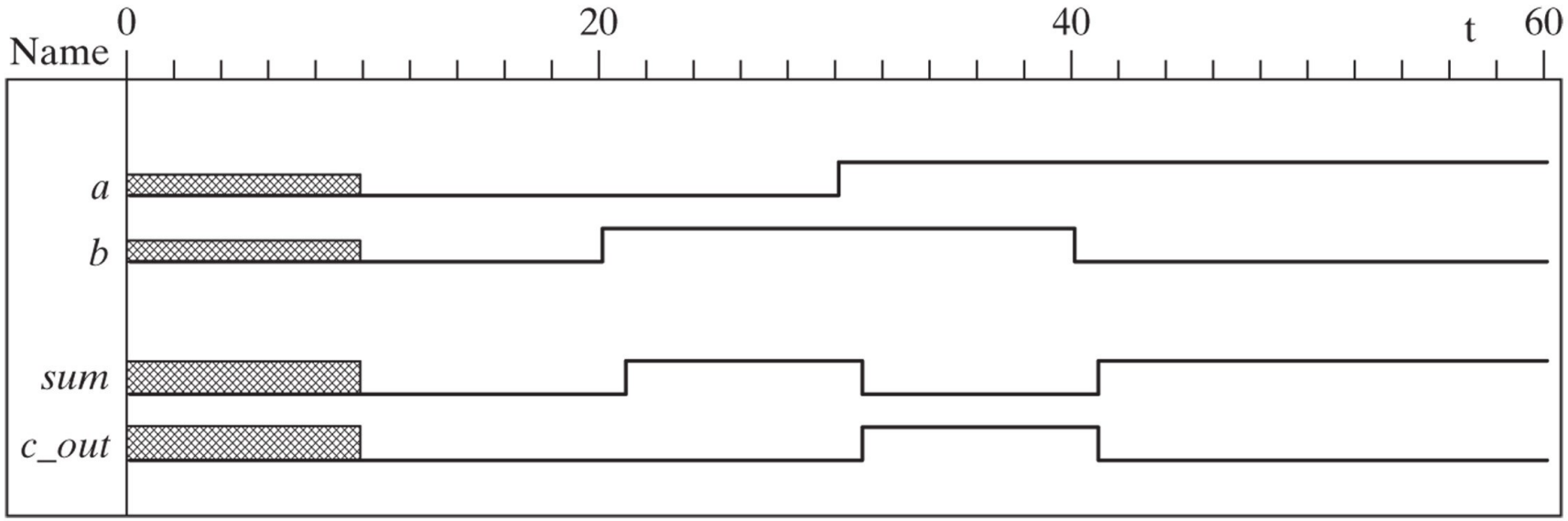
Hierarchical structure of a 4-bit binary comparator



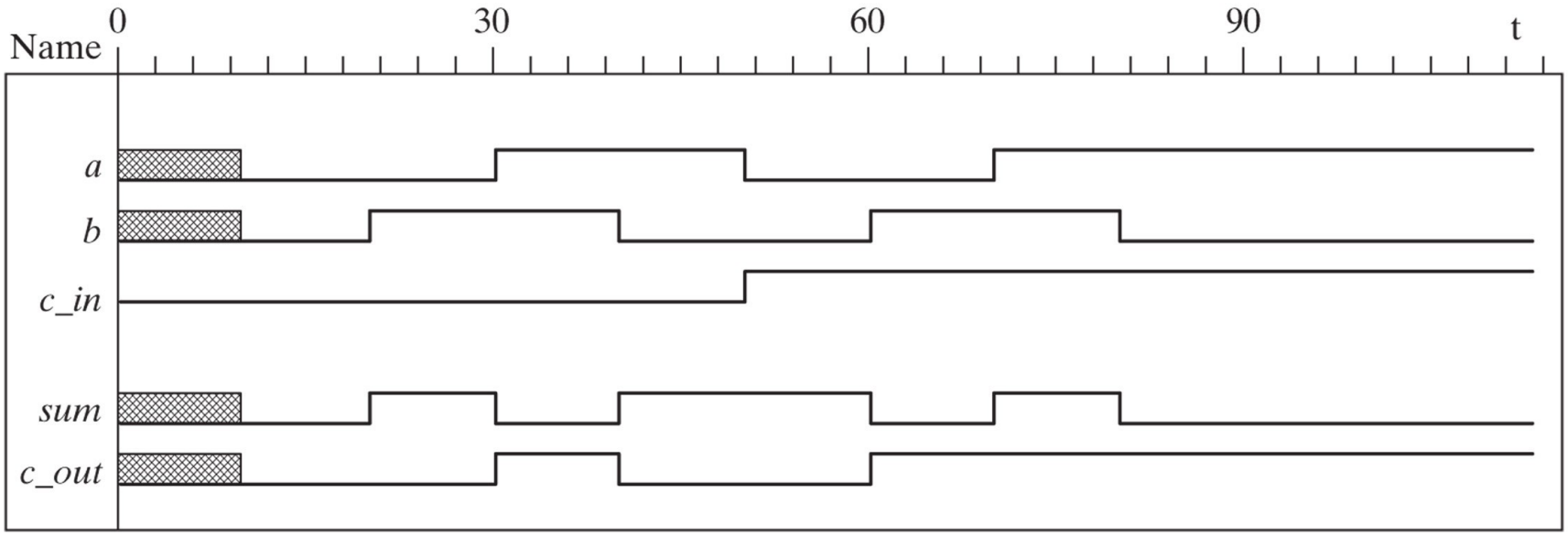
Organization of a testbench for verifying a unit under test.



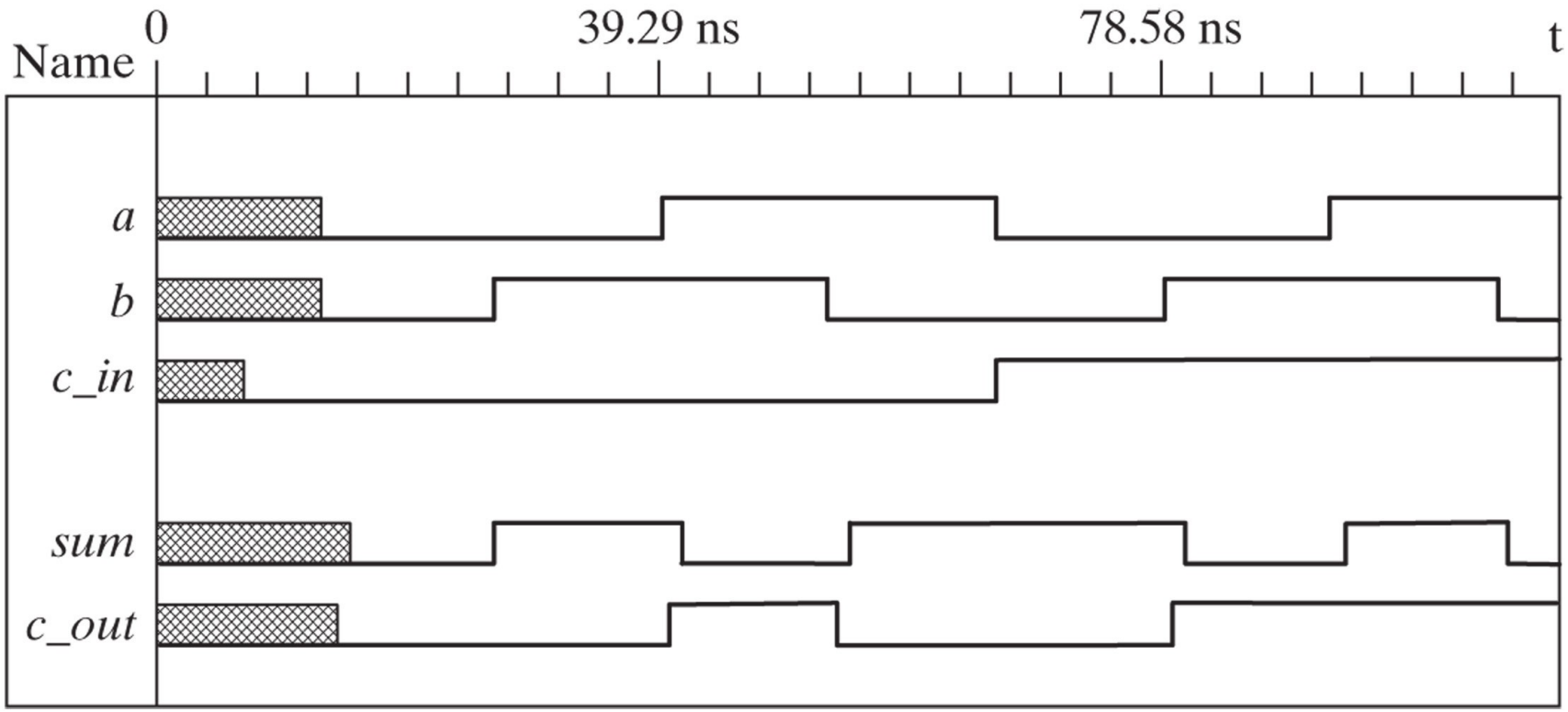
Waveforms produced by a simulation of Add_half , a 0-delay binary half adder.



Results of unit-delay simulation of a 1-bit full adder



Results of simulating a 1-bit full adder implemented with ASIC cells



Final issues

- Please fill out the student info sheet before leaving
- Come by my office hours (right after class)
- Any questions or concerns?