EE4783: HW3

Prob. 1:

Using a cyclic behavior (**always**), write and verify a model of a transparent latch having active high *enable*, and active low *set* and *reset*. The action of *reset* is to drive the output of the latch to 0.

Prob. 2:

Write and verify a behavioral model of J-K flip-flop with active-low asynchronous reset.

Prob. 3:

Write and verify a Verilog model that will assert its output if a 4-bit input word is not a valid binary coded decimal code.