Prob. 1

Using a single continuous assignment, develop and verify a behavioral model implementing a Boolean equation describing the logic of the circuit below. Use the following names for the testbench, the model, and its ports: `t_Combo_CA()`, and `Combo_CA (Y, A, B, C, D)`, respectively. Note: The testbench will have no ports. Exhaustively simulate the circuit and provide graphical and text output demonstrating that the model is correct.

Prob. 2

Write and verify a behavioral model of J-K flip-flop with active-low asynchronous reset.
Prob. 3:

Explain why the code fragment shown below will execute endlessly, and recommend an alternative description.

\begin{verbatim}
reg [3: 0] K
for (K=0; K<=15; K = K+1) begin
...
end
\end{verbatim}

Prob. 4:

15. Write a Verilog description of the circuit shown in Figure P5-15 and verify that the circuit’s output, $P_{odd}$, is asserted if successive samples of $D_{in}$ have an odd number of 1s.

![Circuit Diagram]

Prob. 5

Using continuous assignment statements, develop and verify a model for \texttt{compare_4_32_C4}, a circuit that compares four 32-bit unsigned binary words and asserts output(s) indicating which words have the largest value and which words have the smallest value.