1: (10 pts) Complete the following verilog code for an 8-bit register with synchronous write enable. You may use behavioral verilog.

```
module reg_8b (out, in, we, clk);
    output [7:0] out;
    input [7:0] in;
    input we;
    input clk;
endmodule
```

2: (10 pts) Complete the following verilog code for an 8-bit register with asynchronous write enable. You may use behavioral verilog.

```
module reg_8b (out, in, we, clk);
    output [7:0] out;
    input [7:0] in;
    input we;
    input clk;
endmodule
```
2: (20 pts) Write the Verilog code for a negative edge triggered D flip flop with an active low asynchronous RESET. Name the module `dffrn`. Name the ports (in this order) `Q`, `D`, `CLK`, `RESET`. Write the full module, declaring ALL data types. You chose the period of CLK.
3: (20 pts) Consider the following 2 Verilog modules.

1) Do they have the same function?

2) Sketch the hardware each one implies.
4: (20 pts) Write the Verilog code for the following diagram. Assume negative edge triggered flops, and an active low synchronous reset. Use dataflow modeling (assign statements) for the combinational elements. Use separate procedures for each flop element.
5: (40 pts) Write the Verilog code to implement a device that will shift in serial data and increment a counter every time the pattern 16’hAFAF is found. The counter will reset every 1000 clock cycles. Assume positive edge triggered flop(s) and asynchronous active high reset. The only output of the device will be the counter. The only inputs will be data, clock, and reset. Use normal procedural statements to create the design.
6: (20 pts) Write the full Verilog module that creates 4 flip-flops with the output of the first flop feeding the input of the second flop, the output of the second flop feeding the input of the third flop, and so forth. The ports will be declared as DATA, CLOCK, RESETN, Q. Q will be the output. RESETN is an active low asynchronous reset. The flops are rising edge CLOCK triggered.