Welcome to FPGA 2015!

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FPGA 2015

- Another record year for FPGA attendance:
  - 195 registered (as of last night)
    - Up 7% on 2014, up 15% on 2013
  - Greatest sponsorship to date

- Thanks in particular to:
  - Vaughn Betz, Deming Chen, Mingjie Lin
  - All members of OC, TPC & Best Paper Committee
  - John and Joanne Lateulere

- Program…

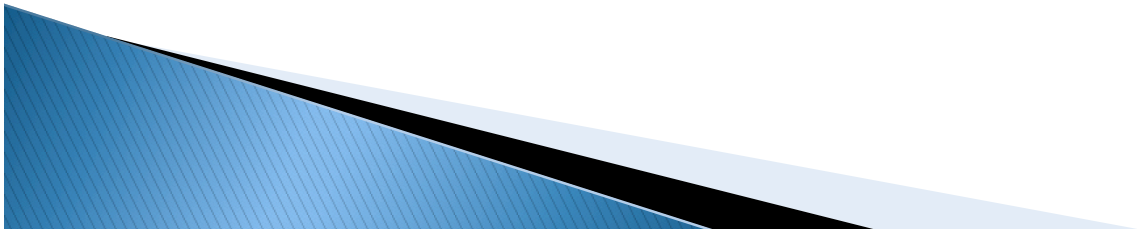
Some Numbers

- 94 submissions to regular research track
  - 36 Applications
  - 18 High-Level Abstractions and Tools for FPGAs
  - 14 FPGA-Based and FPGA-like Computing Engines
  - 9 Architecture
  - 8 CAD
  - 6 Circuit Design
  - 3 Other

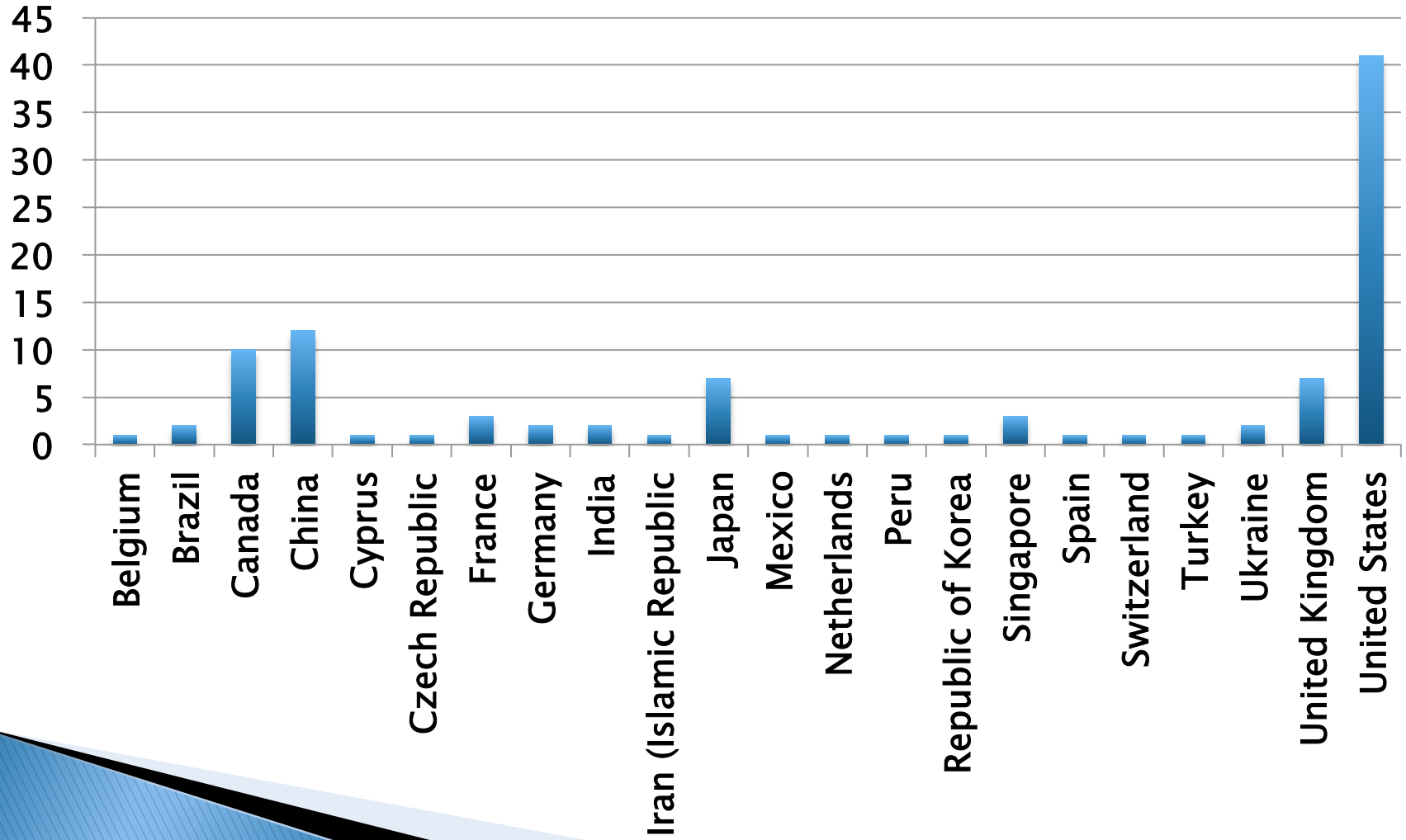
  - 25 short; 69 long

- 8 submissions to designers' track

- 14 submissions from industry or research institutes



From 22 countries



TPC

- Consists of 46 experts from both academia and industry
- Each paper received 5 expert reviews on average
- Held a full-day TPC meeting at Altera for paper selection and program discussion
- A rigorous shepherding process for a small subset of accepted papers for best quality

Paper Acceptance Statistics

- The TPC accepted 20 full and 7 short research papers
  - Acceptance rate is 26%.
- 8 design/tutorial papers
  - A new full-day Designer's Day event
  - A keynote speech
- Four poster sessions
  - A total of 46 additional research projects
  - Short papers will present posters as well

The Program

- Session 1: Computer-aided Design
- Poster Session (1)
- Session 2: Configuration and Processing
- Session 3: Architecture 1
- Poster Session (2)
- Session 4: Architecture 2: Memory Systems
- Banquet and Evening Panel
- Session 5: Processors and Accelerators
- Poster Session (3)
- Session 6: High-level and System-level Synthesis
- Session 7: Circuit Design
- Poster Session (4)
- Session 8: Applications

Three Best Paper Candidates

- **Application of Specific Delay Window Routing for Timing Optimization in FPGA Designs**
- Evan Wegley, Qinhai Zhang (Lattice Semiconductor Corp.)

- **Take the Highway: Design for Embedded NoCs on FPGAs**
- Mohamed S. Abdelfattah, Andrew Bitar, Vaughn Betz (University of Toronto)

- **Optimizing FPGA-based Accelerator Design for Deep Convolutional Neural Networks: An Analytical Approach based on Roofline Model**
- Chen Zhang (Peking University), Peng Li (University of California, Los Angeles), Guangyu Sun (Peking University & University of California, Los Angeles), Yijin Guan (Peking University), Bingjun Xiao (University of California, Los Angeles), Jason Cong (University of California, Los Angeles & Peking University)

Some Logistics

- Authors received emails beforehand for
  - Bio of the presenter
  - Slides for feedback from session chairs
- Long talks: each has a total of 25 minutes
  - 20 minutes for the presentation
  - 5 minutes for Q & A
- Short talks: each has a total of 5 minutes
  - No Q & A
  - A poster in the earliest poster session after the talk
- Please load the latest slides to the conference laptop 15 minutes before the session starts

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