COP 5106 – Fall 2016 - Homework 2

Due: November 28, 2016

**Instructions:**

* Submit your answers in the form of a single document file
* Include the flow of the reasoning and calculations in the text.
* Remember that the homework is **individual** work.

**Problem 1:**

Consider an SMP system with two processors A and B using the MSI snoopy cache coherence protocol. Assume we have memory location X addressed by the two processors. In the following table, you see the series of memory accesses by the two processors. Fill in the remainder of the table similarly to the first three rows.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Processor activity | Bus activity | Content of Proc A’s cache | Contents of Proc B’s cache | Contents of mem location X |
| A reads X | Read miss | X=0 (shared) | X=invalid | 0 |
| B reads X | Read miss | X=0 (shared) | X=0 (shared) | 0 |
| A reads X | Read hit | X=0 (shared) | X=0 (shared) | 0 |
| A writes X=2 |  |  |  |  |
| B reads X |  |  |  |  |
| B writes X=3 |  |  |  |  |
| A writes X=4 |  |  |  |  |

**Problem 2:**

Let us consider a NUMA system using directory based cache coherence. Let us assume that there are two processors:

* Proc A, which has memory locations M=#A000 - #AFFF, cache A and directory A
* Proc B, which has memory locations M=#B000 - #AFFF, cache B and directory B

Assume all memory locations are initialized to 0. The events creates by a memory access can be traced as follows:

**1. Proc A reads memory location #B001**

Messages:

 Message “Read Miss” from Cache A to Directory B: (A, #B001)

 Message “Data value reply” from Directory B to Cache A: value = 0

Results

 Memory B: value at #B001 = 0

 Directory B: State of #B001 = Shared, sharers {A}

 Cache A: Value of #B001 = 0

Trace the following events:

2. Proc A reads memory location #A001

3. Proc B reads memory location #B001

4. Proc A writes memory location #B001 with 2

5. Proc A reads memory location #A001

6. Proc B writes memory location #B001 with 3